


# Testing Digital Systems II

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## Lecture 6: Built-in Self Test (II)

Instructor: M. Tahoori

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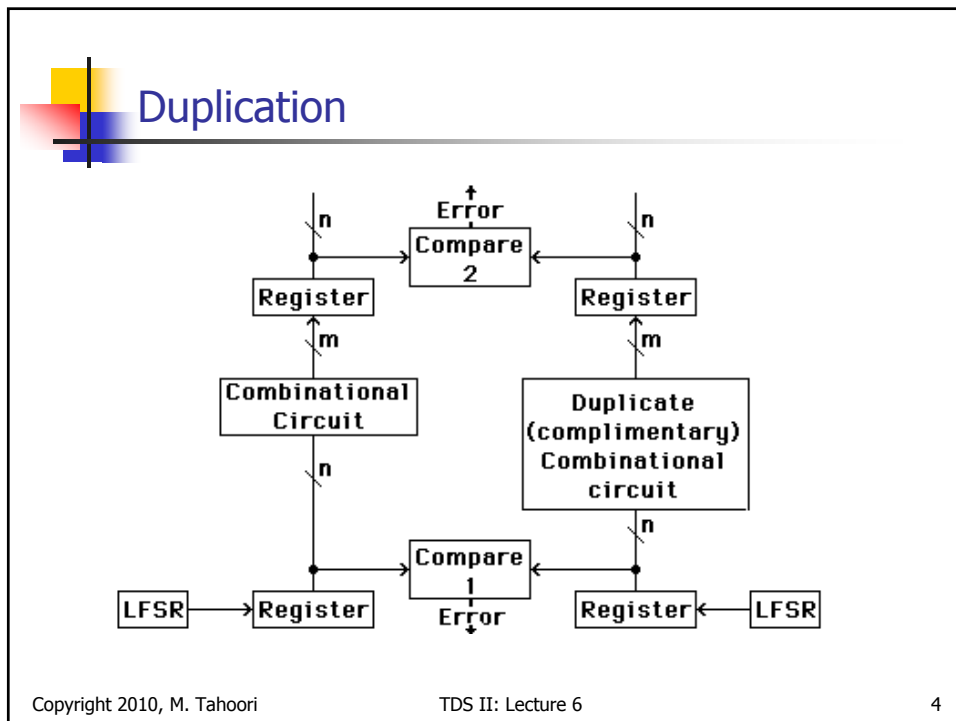
## Output Response Analyzer

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## Output Response Analysis

- Duplication
- Response Compaction
  - Parity, Transition, Ones Counting
  - Syndrome Analysis, Checksums
  - Walsh Coefficients — Spectral Techniques
  - Signature Analysis — Galois Division using an LFSR

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## Parity

- Parity testing
  - Detects all single bit and multiple bit errors of odd cardinality

$P(X) = X + 1$

$$P = \sum_{i=1}^L r_i$$

where  $L$  is the length of the test.

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## Ones Count Testing

Assume the CUT has one output and the output contains a stream of  $L$  bits. Let the fault-free output response be

$$\{r_0, r_1, r_2 \dots r_{L-1}\}$$

Ones count testing will need a counter to count the number of 1s in the bit stream.

**Aliasing probability [Savir 1985]**

$$P_{oc}(m) = (C(L, m) - 1) / (2^L - 1)$$

L bit output sequence containing m ones

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## Ones Counting

- One Counting :
  - # of 1's in the response stream is compared with fault free value

```

    graph LR
      A[test patterns] --> B[CUT]
      B --> C[Counter]
      style A fill:none,stroke:none
      style C fill:none,stroke:none
    
```

- For the fault-free circuit, the 1-count is 5.
  - The faults a/0 and a/1 would be detected since the counts would be 4 and 6.

```

    graph LR
      a[11110000] --- AND1[AND]
      b[11001100] --- AND1
      c[10101010] --- AND1
      AND1 --- out[11000000]
    
```

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## Transition Count Testing

Transition count testing is similar to that for ones count testing, except the signature is defined as the number of *1-to-0* and *0-to-1* transitions.

*[Hayes 1976]*

**Aliasing probability**

$$P_{TC}(m) = (2C(L-1, m) - 1) / (2^L - 1)$$

L bit output sequence containing m transitions

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## Transition Counting

- **Transition Count Response Compaction**
  - Count # transitions from 0→1 and 1→0 as a signature

(a) Logic simulation of good machine and fault a stuck-at-1.

(b) Transition counts of good and failing machines.

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## Transition Counting Details

- Transition count:
  - $C(R) = \sum_{i=1}^m (r_i \oplus r_{i-1})$  for all  $m$  primary outputs
  - To maximize fault coverage:
    - Make  $C(R_0)$  – good machine transition count – as large or as small as possible

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## Signature Analysis

- Definition:
  - *Signature* is Remainder in LFSR after Galois Division of Test Output Bit Stream
- Aliasing Definition and Coverage Loss Demonstration
- Division Examples
- Linearity Demonstration
- Aliasing Analysis and Design Guidelines
- Multiple-Output DUT
  - Multiplexed Outputs
  - Parallel Signature Analysis (aka MISR)
  - Masking in Parallel Signature Analyzer

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## Serial Signature Analyzer

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## Signature Analysis

- Definition:
  - *Signature* is Remainder in LFSR after Galois Division of Test Output Bit Stream

- LFSR Polynomial:  $1+X^2+X^3$
- Test Output Data =  $00011 = X^3+X^4$
- Signature =  $010 = X$  (remainder of  $X^3+X^4 \div 1+X^2+X^3$ )
  - (Assumes 000 Initial Contents)
- *Serial Signature Analysis*
  - One Test Output Data Stream

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## Signature Analysis

- Why is It Used?
  - Reduce Amount of Stored Test Data
- When is It Used?
  - Usually for Built-In Self Test
- What are Its Drawbacks?
  - Possible Loss of Effective Fault Coverage
    - Aliasing
      - Signature (Fault Present) = Signature (Fault Free)
    - Masking

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### Stuck-Fault Error Pattern Example

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### Alias Example

$X^3$ Fault-Free		$X^2+1$
$X^3+X^4$ Input S-a-1		$X$
$1+X+X^2+X^3+X^4$ Output S-a-1		$X^2+1$
$1+X+X^2+X^4$ Output S-a-1 Error		$0$

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### Linearity Example

The diagram shows three instances of a 3-bit LFSR. Each instance has an input sequence and an output sequence. The LFSR consists of three flip-flops with feedback connections. The feedback is taken from the output of the second flip-flop and XORed with the output of the third flip-flop. The feedback result is then XORed with the output of the first flip-flop to produce the next input to the first flip-flop.

Input Sequence	Output Sequence
00010	000
11001	101
11011	100

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### Alias Example

The diagram shows a 3-bit LFSR with an input sequence of 10011. The LFSR consists of three flip-flops with feedback connections. The feedback is taken from the output of the second flip-flop and XORed with the output of the third flip-flop. The feedback result is then XORed with the output of the first flip-flop to produce the next input to the first flip-flop.


$H(z) = 1011$

Input sequence: 1 0 0 1 1

Output sequence: 1 0 0 1 1

- Signature  $[H] = 0$  ( $H$  is LFSR generating polynomial)
- Signature  $[G \times H] = 0$  for any polynomial  $G$
- $Z_{\text{Faulty}} = Z_{\text{Fault-Free}} + Z_{\text{Error}}$
- $Z_{\text{Error}} = G \times H \Rightarrow \text{Signature}[Z_{\text{Faulty}}] = \text{Signature}[Z_{\text{Fault-Free}}]$

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## Determining Effective Fault Coverage

- **Approach 1:**
  - Include signature analysis in fault grading simulation
    - Precludes fault dropping in simulation
      - Can be prohibitively expensive
- **Approach 2:**
  - Retain intermediate signatures during test
    - Allows fault dropping in simulation
      - Requires storage of intermediate signatures
      - Requires interruption of test process
- Both approaches costly, no insight into design


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## Design Issues

- What LFSR for Signature Register?
  - How Many Stages?
  - What Feedback Connections?
    - 2 Primitive or Non-Primitive Polynomial


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## Alias Probability Bound

- Serial Signature Analysis
  - $L_c$ : # patterns generated by LFSR
  - $L$ : test length
- Alias Probability  $\leq (1 + \varepsilon) / L$        $L < L_c$ 
  - $\varepsilon < 1$ , small for large  $L$ 
    - Example:  $\varepsilon = 0.04$  for  $L=1000$
- Alias Probability  $\leq 1$     $L = hL_c$
- Alias Probability  $\leq 2/(L_c+1)$     $L > L_c$  ,  $L \neq hL_c$

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## Serial Signature Analysis

- Which Polynomial?
  - Primitive Maximizes  $L_c$  for Given  $r$
- Exact Aliasing Not Monotonic
- Conjecture: Best Monotonic Bound =  $1/L$
- Guideline:
  - Use Signature Polynomial with Period  $>$  Test Length.
  - Example (Serial Signatures)
    - $L=10^6$ , Primitive Polynomial,  $r \geq 20$
    - Alias Probability  $< 0.0001$  %

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## Multiple Output Circuits

(a)                      (b)                      (c)                      (d)


SSA = Serial Signature Analyzer    PSA = Parallel Signature Analyzer or MISR

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## Parallel signature Analyzer

- aka MISR or Multiple-Input Signature Register


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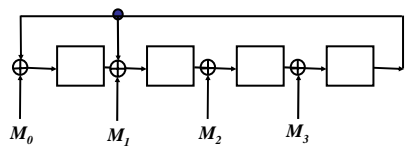
## Multiple-Input Signature Register

- This scheme is equivalent k single input SAs
  - but with the input stream shifted in time
  - $Z(X) = Z_1(X) + XZ_2(X) + \dots + X^k Z_{k+1}(X)$ .
- The error polynomial of the four outputs
  - $E(X) = E_1(X) + XE_2(X) + X^2 E_3(X) + X^3 E_4(X)$

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## 4-stage MISR



$M_0$     $M_1$     $M_2$     $M_3$

$M_0$	1	0	0	1	0
$M_1$	0	1	0	1	0
$M_2$	1	1	0	0	0
$M_3$			1	0	0
$M$	1	0	0	1	1

*A 4-stage MISR*

*An equivalent M sequence*

**Aliasing probability**

$$P_{PSA}(n) = (2^{(mL-n)} - 1) / (2^{mL} - 1)$$

mL-bit sequences to be compacted in n-stage MISR,  $L > n \geq m \geq 2$   
 For  $L \gg n$ ,  $P_{PSA}(n) \approx 2^{-n}$

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## Masking

- What is Masking?
  - Error Bit in One Output CANCELS
    - Error Bit in Another Output
  - Errors in  $Z_j$  at time  $t$  and in  $Z_{j+m}$  at time  $t + m$  Cancel One Another

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## Signature Analysis

- Serial Signature Analysis
  - Coverage Loss due to Aliasing
    - Use Primitive Polynomial?
    - Use Longer Register?
    - Use Multiple Registers?
- Parallel Signature Analysis (aka MISR)
  - Coverage Loss due to Aliasing and Masking
    - Use Primitive Polynomial?
    - Use Longer Register?
    - Use Multiple Registers?
    - Use Checksum along with Signature?

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