


Testing Digital Systems II

Lecture 4: External Scan Techniques IEEE 1149.1 : JTAG

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Purpose of Standard

- Originally a DFT technique for PCBs
- Lets test instructions and test data be serially fed into a *component-under-test* (CUT)
 - Allows reading out of test results
- JTAG can operate at chip, PCB, and system levels
- Allows control of tri-state signals during testing
- Lets other chips collect responses from CUT
- Lets system interconnect be tested separately from components
- Lets components be tested separately from wires

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Basic Idea of Boundary Scan

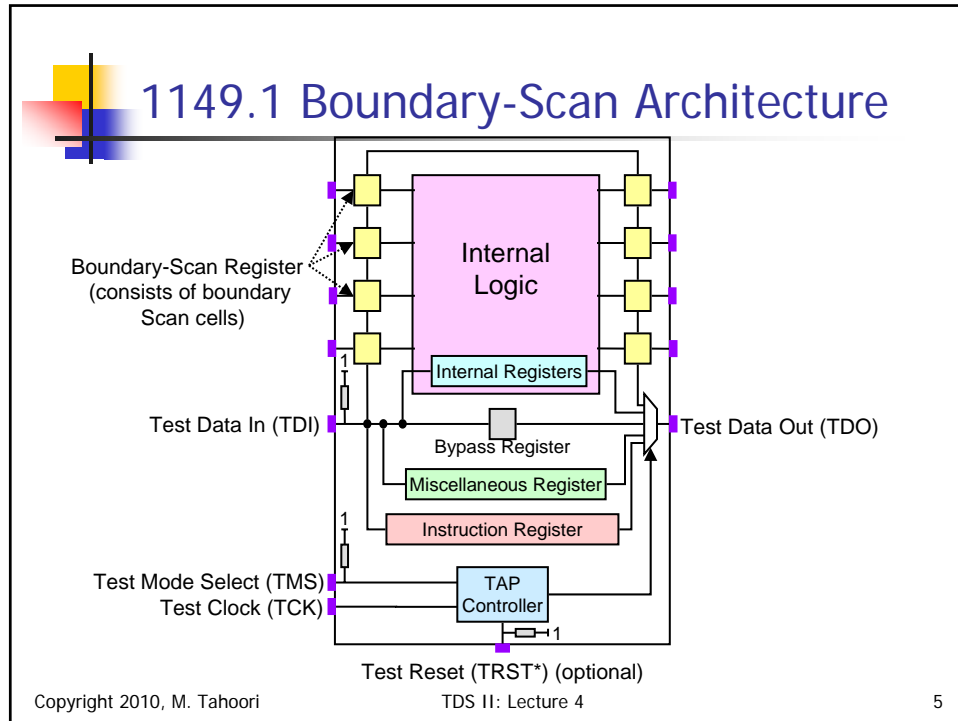
The diagram illustrates a single boundary-scan cell. It consists of a central yellow box labeled "Internal Logic". Surrounding this logic is a ring of eight cyan square flip-flops. The top four flip-flops are connected in a series, with an arrow pointing from left to right. The bottom four flip-flops are also connected in a series, with an arrow pointing from right to left. This configuration forms a closed loop around the internal logic. Labels "Boundary-scan cell" and "Internal Logic" are present.

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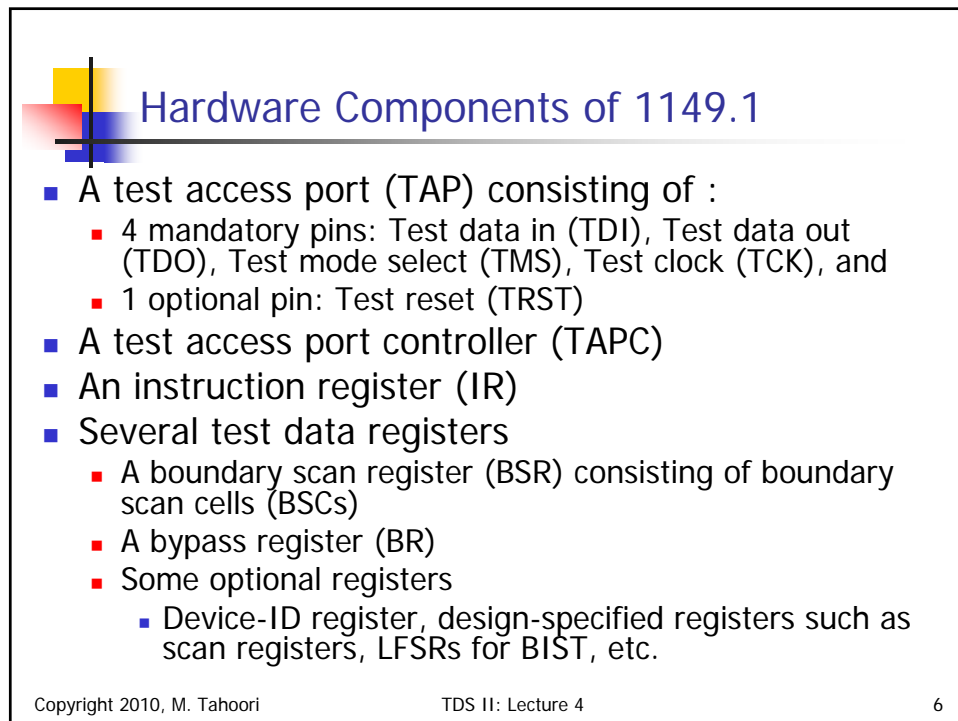
A Board Containing 4 IC's with Boundary Scan

The diagram shows a board with four ICs arranged in a 2x2 grid. Each IC contains "Internal Logic" (yellow box) and a "Boundary-scan chain" (cyan flip-flops). The top-left IC has a "Serial Data in" input. The bottom-left IC has a "Serial Data out" output. A "System interconnect" line runs horizontally across the bottom of the board, connecting to the bottom of each IC. Labels "Boundary-scan cell", "Boundary-scan chain", "Internal Logic", "Serial Data in", "Serial Data out", and "System interconnect" are present.

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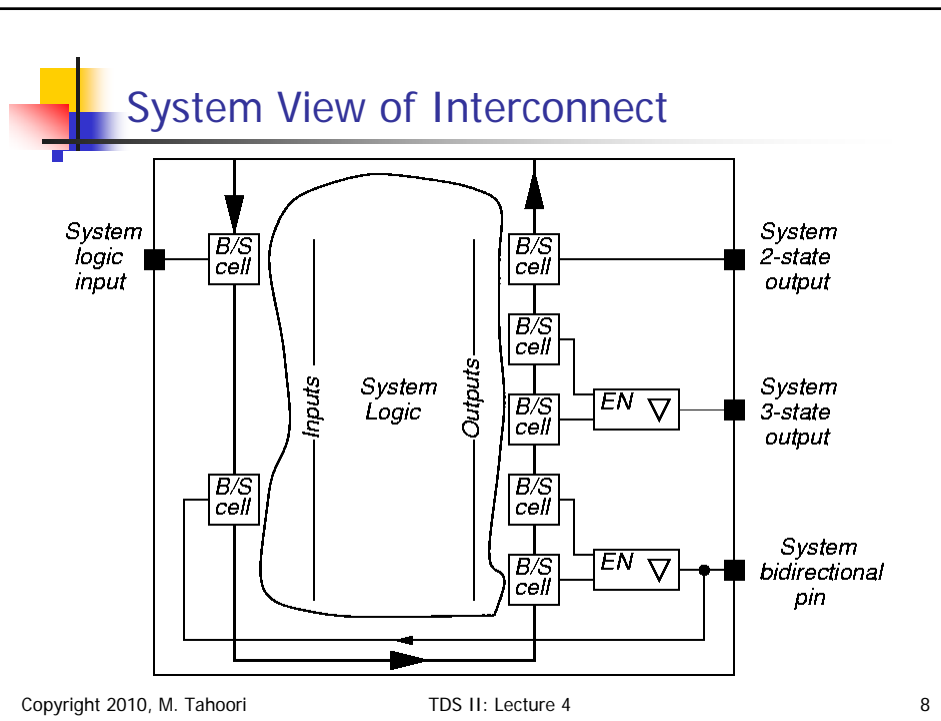
Basic Operations

1. Instruction sent (serially) through TDI into instruction register.
2. Selected test circuitry configured to respond to the instruction.
3. Test pattern shifted into selected data register and applied to logic to be tested
4. Test response captured into some data register
5. Captured response shifted out; new test pattern shifted in simultaneously
6. Steps 3-5 repeated until all test patterns are applied.

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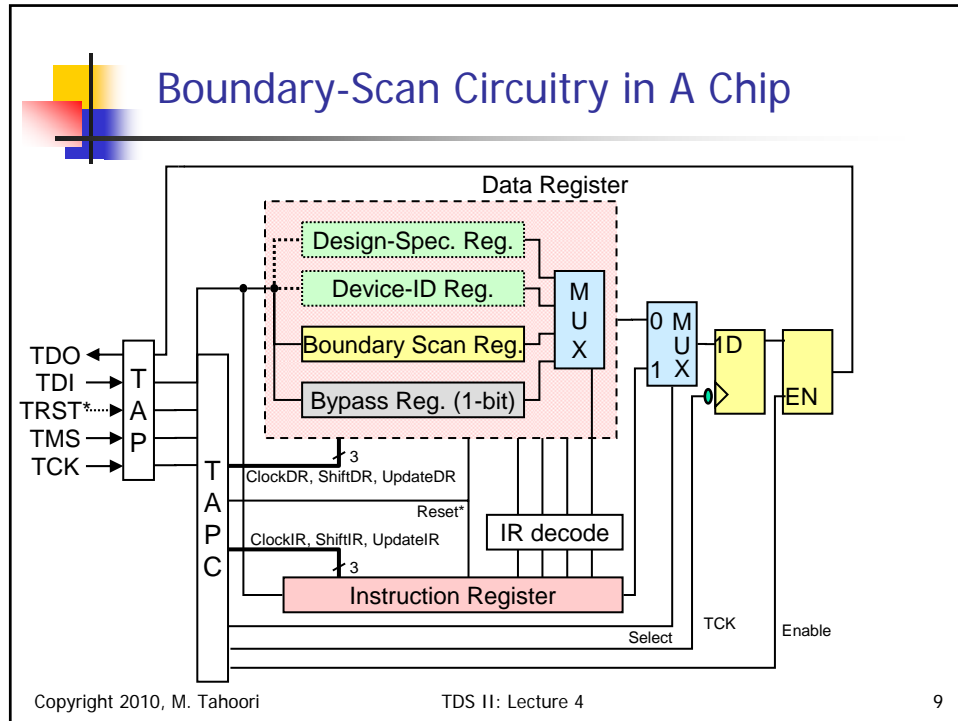
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Data registers

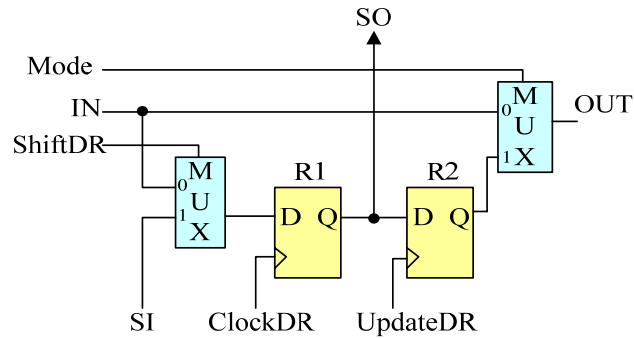
- Boundary scan register: consists of boundary scan cells
- Bypass register: a one-bit register used to pass test signal from a chip when it is not involved in current test operation
- Device-ID register: for the loading of product information (manufacturer, part number, version number, etc.)
- Other user-specified data registers (scan chains, LFSR for BIST, etc.)

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A Typical Boundary-Scan Cell (BSC)



- Operation modes
 - Normal: IN → OUT (Mode = 0)
 - Shift: TDI → ... → IN → OUT → ... → TDO (ShiftDR = 1, ClockDR)
 - Capture: IN → R1, OUT driven by IN or R2 (ShiftDR = 0, ClcokDR)
 - Update: R1 → OUT (Mode_Control = 1, UpdateDR)

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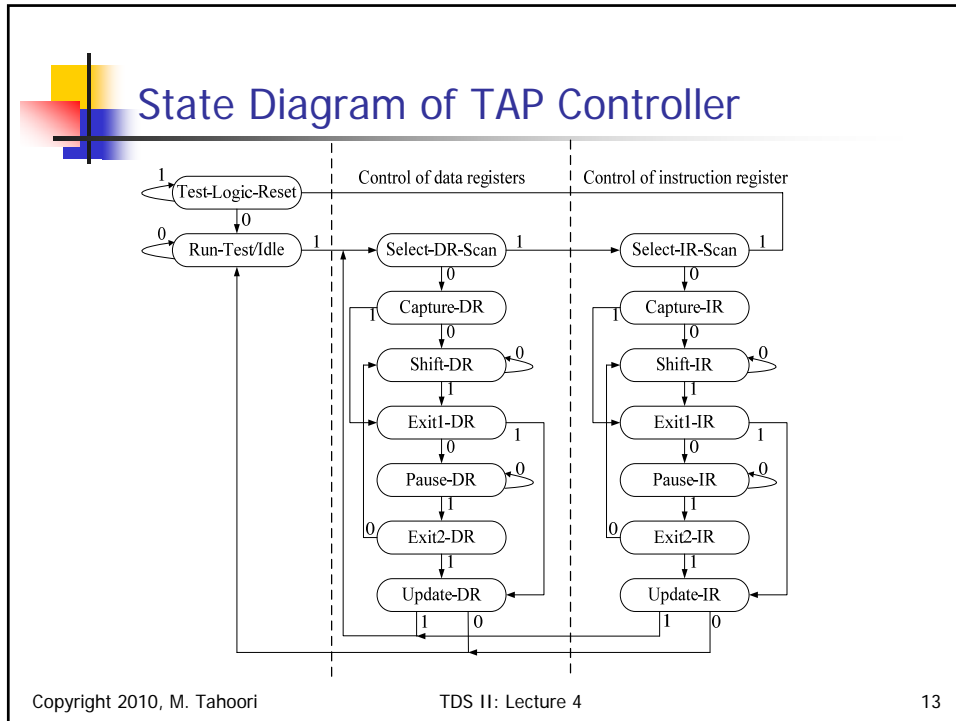
TAP Controller

- A finite state machine with 16 states
- Input: TCK, TMS
- Output: 9 or 10 signals included ClockDR, UpdateDR, ShiftDR, ClockIR, UpdateIR, ShiftIR, Select, Enable, TCK and TRST* (optional).


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- ### Main functions of TAP controller
- Providing control signals to
 - Reset BS circuitry
 - Load instructions into instruction register
 - Perform test capture operation
 - Perform test update operation
 - Shift test data in and out
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States of TAP Controller

- Test-Logic-Reset: normal mode
- Run-Test/Idle: wait for internal test such as BIST
- Select-DR-Scan: initiate a data-scan sequence
- Capture-DR: load test data in parallel
- Shift-DR: load test data in series
- Exit1-DR: finish phase-1 shifting of data
- Pause-DR: temporarily hold the scan operation (e.g., allow the bus master to reload data)
- Exit2-DR: finish phase-2 shifting of data
- Update-DR: parallel load from associated shift registers
- **Note: Controls for IR are similar to those for DR.**

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Instruction Set

- BYPASS
 - Bypass data through a chip
- SAMPLE
 - Sample (capture) test data into BSR
- PRELOAD
 - Shift-in test data and update BSR
- EXTEST
 - Test interconnection between chips of board
- Optional
 - INTEST, RUNBIST, CLAMP, IDCODE, USERCODE, HIGH-Z, etc.

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BYPASS Instruction

- Purpose: Bypasses scan chain with 1-bit register

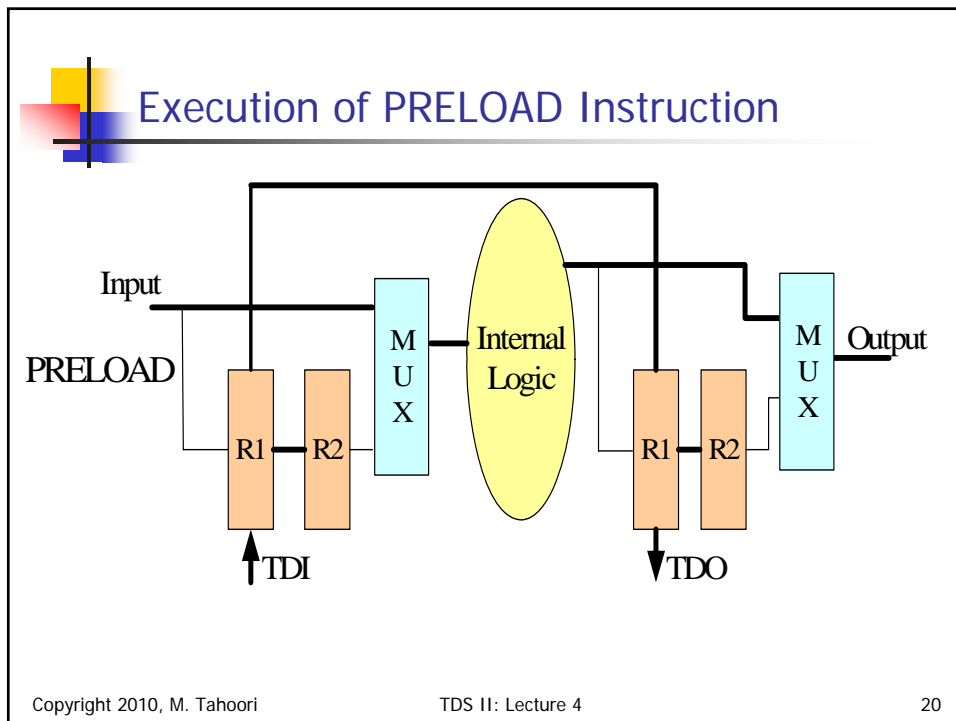
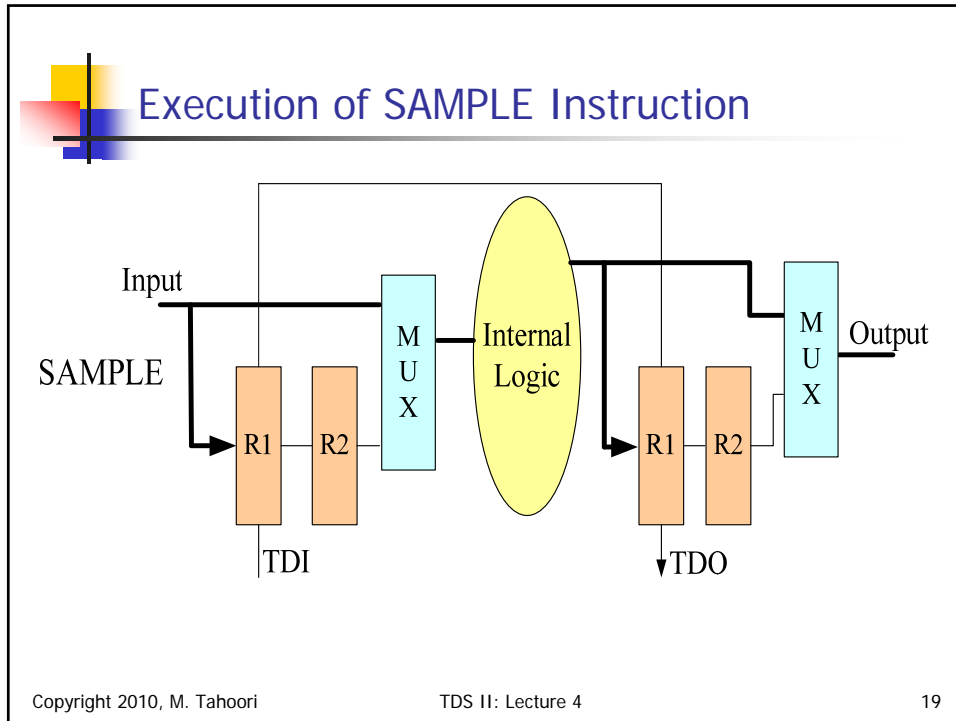
The diagram shows a 1-bit register with inputs *TDI* and *ShiftDR* connected to an AND gate, whose output is the *D* input of the register. The *ClockDR* signal is connected to the *CLK* input. The *Q* output of the register is labeled *To TDO*. Below, a scan chain of three ICs (IC56, IC57, IC58) is shown. IC57 is highlighted with a blue border, indicating it is bypassing the scan chain.

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Execution of BYPASS Instruction

The diagram illustrates the internal components of a TAP Controller during the execution of a BYPASS instruction. It includes an *Internal Logic* block, a *Bypass Register (1 bit)*, an *Instruction Register*, and a *TAP Controller* block. The *TAP Controller* receives *TMS* and *TCK* signals and outputs *TRST*. The *Bypass Register (1 bit)* receives *TDI* and outputs *TDO*. The *Instruction Register* is also connected to the *TAP Controller*.

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Execution of EXTEST Instruction (1/3)

- Shift-DR (Chip1)

The diagram shows two identical chips connected via JTAG. Each chip contains an Internal Logic block, a Registers block, and a TAP controller block. The TAP controller of the first chip is connected to the TAP controller of the second chip. The TDI and TDO pins are also connected between the two chips.

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Execution of EXTEST Instruction (2/3)

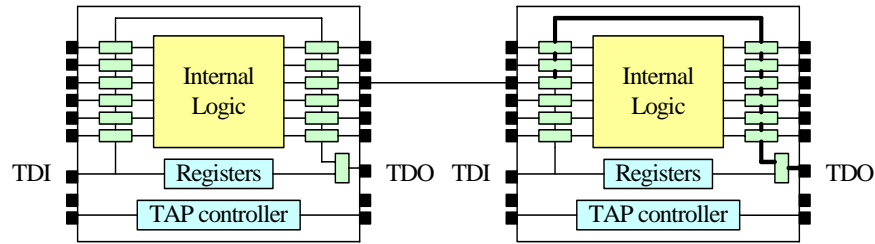
- Update-DR (Chip1)
- Capture-DR (Chip2)

The diagram shows two identical chips connected via JTAG. Each chip contains an Internal Logic block, a Registers block, and a TAP controller block. The TAP controller of the first chip is connected to the TAP controller of the second chip. The TDI and TDO pins are also connected between the two chips.

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Execution of EXTEST Instruction (3/3)

- Shift-DR (Chip2)



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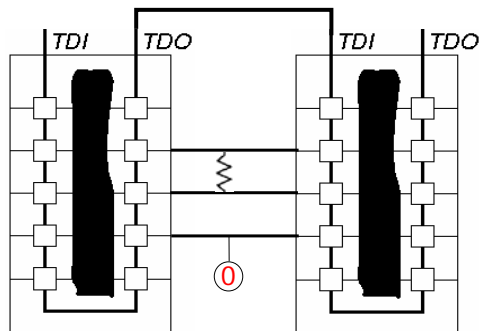
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External Test

- Example of testing interconnects

- Input: X X X X X X **1 0 1** X X X X X X X X X X
- Output: X X X X X X X X X X X **0 0 0** X X X X X X



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Execution of INTEST Instruction (1/4)

- Shift-DR

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Execution of INTEST Instruction (2/4)

- Update-DR

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Execution of INTEST Instruction (3/4)

- Capture-DR

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Execution of INTEST Instruction (4/4)

- Shift-DR

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Internal Test

- Example of testing chip logic
 - Input: X 1 0 X X X X X X X
 - Good output: X 0 X X X X X X X X

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RUNBIST Instruction

- Purpose:
 - Allows to issue BIST command to component through JTAG hardware
- Optional instruction
- Lets test logic control state of output pins
 - Can be determined by pin boundary scan cell
 - Can be forced into high impedance state
- BIST result (success or failure) can be left in boundary scan cell or internal cell
 - Shift out through boundary scan chain
- May leave chip pins in an indeterminate state (reset required before normal operation resumes)

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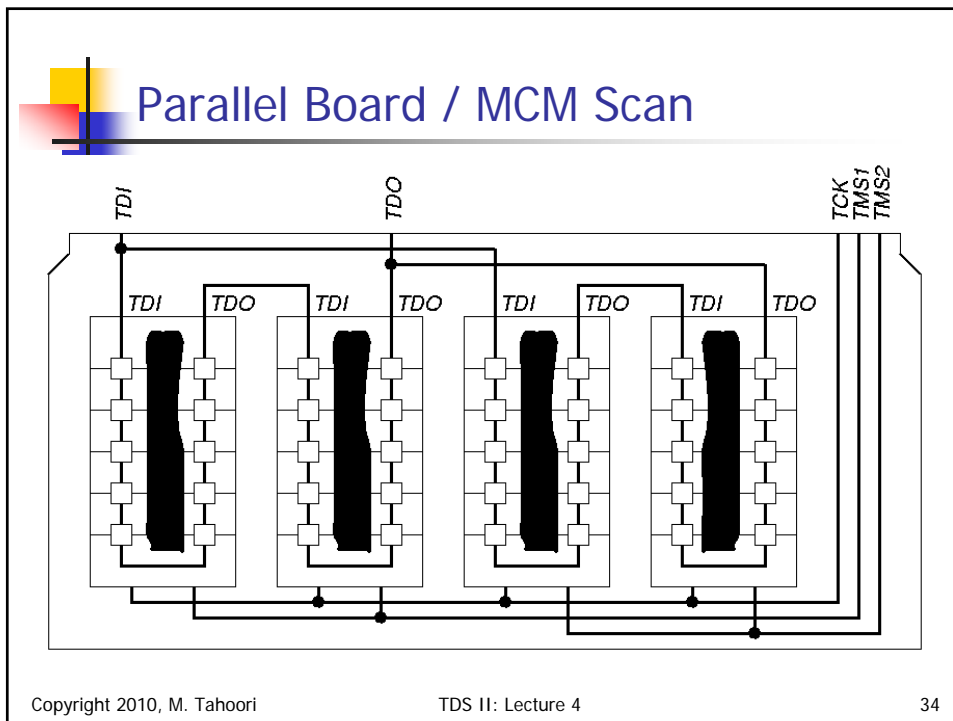
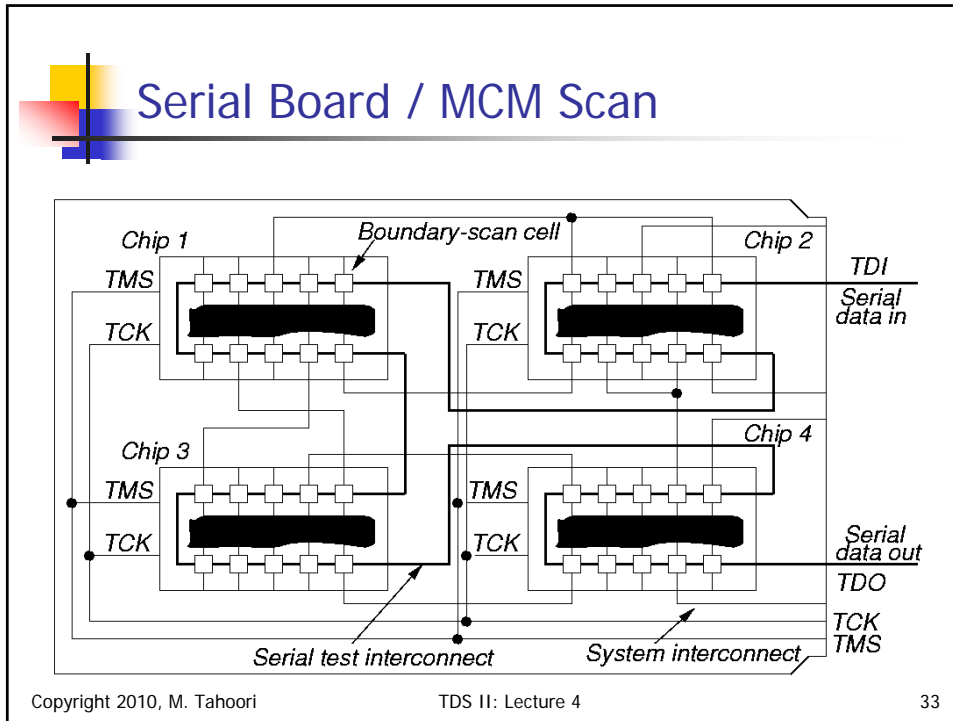
IDCODE Instruction

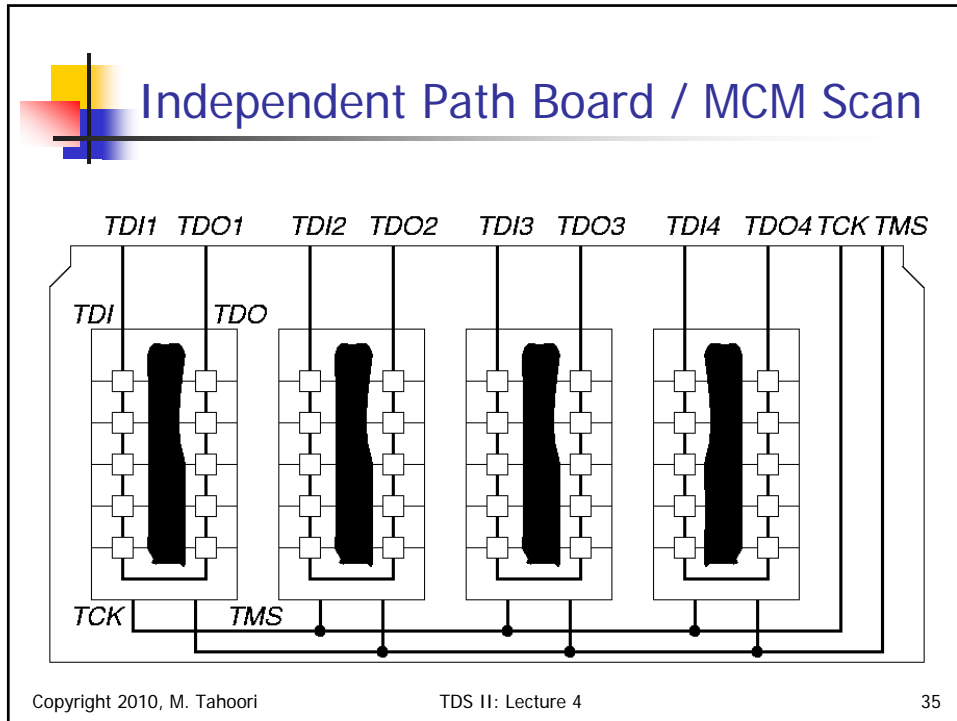
- Purpose: Connects the component device identification register serially between *TDI* and *TDO*
 - In the *Shift-DR* TAP controller state
- Allows board-level test controller or external tester to read out component ID
- Required whenever a JEDEC identification register is included in the design



Optional / Required Instructions

Instruction	Status
<i>BYPASS</i>	Mandatory
<i>CLAMP</i>	Optional
<i>EXTEST</i>	Mandatory
<i>HIGHZ</i>	Optional
<i>IDCODE</i>	Optional
<i>INTEST</i>	Optional
<i>RUNBIST</i>	Optional
<i>SAMPLE / PRELOAD</i>	Mandatory
<i>USERCODE</i>	Optional





Summary

- Boundary Scan Standard has become absolutely essential
 - No longer possible to test printed circuit boards with *bed-of-nails* tester
 - Not possible to test multi-chip modules at all without it
 - Supports BIST, external testing with Automatic Test Equipment, and boundary scan chain reconfiguration as BIST pattern generator and response compacter
 - Now getting widespread usage

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