Testing Digital Systems II

Lecture 3:
Design for Testability (II)

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Scan Architecture

Structured DFT

- Difficulty with the ad hoc testability techniques
  - The requirement of adding extra control inputs or observation outputs
- Structured DFT techniques
  - Permit access to internal nodes of a circuit without requiring a separate external connection for each node accessed
  - At the cost of additional internal logic circuitry used primarily for testing

Scan Features

- Very few (from 1 to 4) additional external connections are used to access many internal nodes
  - Typically all of the system bistable elements
- Serialization of the test data
  - Otherwise, a large number of I/O pins will be required to control and observe logic values stored in each system bistable
- Test data must be transferred serially or *scanned* in and out of the circuit being tested.
- The change from normal system operation to test mode can be controlled by a level test-mode signal or by a separate test clock signal

Scan Features

- Most important advantage
  - <u>sequential circuit test pattern generation is not required</u>
  - Test pattern generation need only be done for the combinational circuits
    - the bistable elements can be accessed and tested directly
- converting between parallel and serial data
  - Two approaches
    - shift register (scan-path method)
    - multiplexer

Scan Design

- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design:
  - Add a *test control* (TC) primary input.
  - Replace flip-flops by *scan flip-flops* (SFF) and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.
- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.
- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.

Scan Design Rules

- Use only clocked D-type of flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
- Clocks must not feed data inputs of flip-flops.

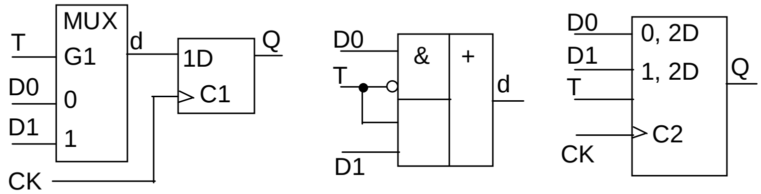
Scan Path Method

- Circuit with two modes of operation
  - Normal functional mode
  - Test mode
    - Circuit bistables are interconnected into a shift register
- With the circuit in test mode
  - It is possible to shift an arbitrary test pattern into the bistables
- By returning the circuit to normal mode for one clock period
  - The combinational circuitry acts upon the bistable contents and primary input signals,
  - Stores the results in the bistables
- Circuit is then placed into test mode
  - It is possible to shift out the contents of the bistables and
  - Compare these contents with the correct response

Scan Path Methods for Flip-Flop Machines

Scan Path Methods for Flip-Flop Machines

- Each of the circuit flip-flops is replaced by
  - Multiplexed data flip-flop (MD flip-flop)



(a) (b) (c)

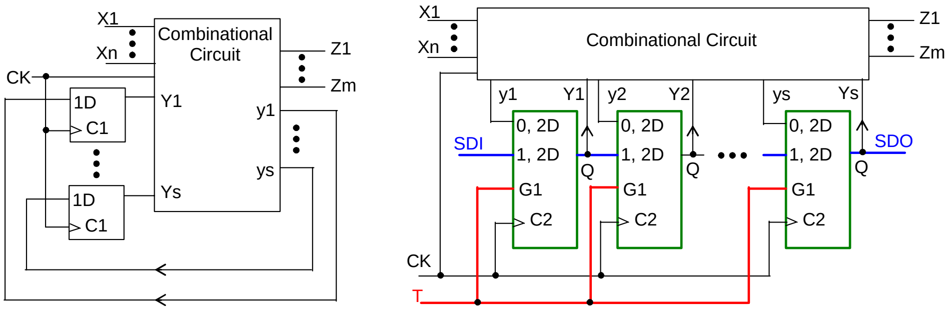
- (a) flip-flop with multiplexer (MUX)
- (b) multiplexer circuit diagram
- (c) symbol for multiplexed data flip-flop (MD flip-flop)

MD Flip-flop Architectures

- A multiplexer is placed at the data input of a flip-flop
  - To permit a selection of two different data inputs
    - d0: (normal system operation)
    - d1: (test mode).
- The choice of data input is based on the value of the control input, T.
  - When T=0, data is gated from the d0 input upon an active clock transition.
  - Data is taken from d1 if T is equal to 1.

MD Flip-flop Architectures

- (a) General structure of a flip-flop finite state machine
- (b) MD-flip-flop scan path architecture



(a)

(b)

MD Full-Scan Design

- *Primary inputs* (PIs)
  - the external inputs to the circuit
  - can be set to any required logic values
  - set directly in parallel from the external inputs
- *Pseudo primary inputs* (PPIs)
  - the scan cell outputs
  - can be set to any required logic values
  - are set serially through scan chain inputs
- *Primary outputs* (POs)
  - the external outputs of the circuit
  - can be observed
  - are observed directly in
  - parallel from the external outputs
- *Pseudo primary outputs* (PPOs)
  - the scan cell inputs
  - can be observed
  - are observed serially through scan chain outputs

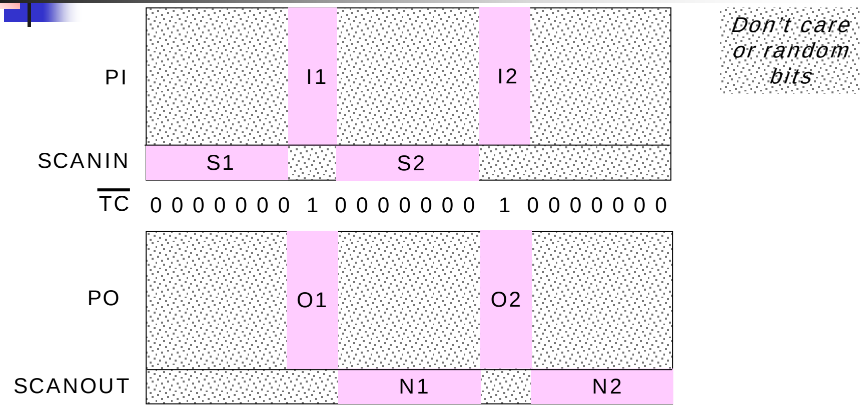
MD Flip-flop Architectures

- general structure of a flip-flop finite state machine
  - CK is the clock input,
  - $X1, \ldots, Xn$ are the primary inputs
  - $Z1, \ldots, Zm$ are the primary outputs.
  - There are *s* D-flip-flops corresponding to internal variables $y1, \ldots, ys$.
- scan path architecture using MD flip-flops
  - One additional input, the T input, has been added
  - T = 0: The upper data inputs $(y1, \ldots, ys)$ act as the flip-flop *D* inputs
  - T = 1: The lower data inputs become the flip-flop *D* inputs.
    - $D_i = Q_{i-1}$ for i from 2 to *s*, and a shift register is formed
      - The primary input Xn is connected to D1 becoming the shift register input
      - Qs, the shift register output, appears at the primary output Zm.

Testing of the combinational logic

1. Setting T = 1 (scan mode)
2. Shifting the test pattern y_j values into the flip-flops.
3. Setting the corresponding test values on the Xi inputs.
4. Setting T = 0 and, after a sufficient time for the combinational logic to settle, checking the output Z_k values.
5. Applying a clock signal to *CK*.
6. Setting T = 1 and shifting out the flip-flop contents via Z_m.
    - The next y_j test pattern can be shifted in at the same time.
    - The y_j values shifted out are compared with the good response values for y_j.

Testing of the combinational logic



Sequence length = (n_{comb} + 1) n_{sff} + n_{comb} *clock periods*

n_{comb} = number of combinational vectors

n_{sff} = number of scan flip-flops

Testing Flip-Flops in Scan Chain

- Scan register must be tested prior to application of scan test sequences
- To verify the possibility of shifting both a 1 and a 0 into each flip-flop
  - Shifting a string of 1s and then a string of 0s through the shift register
  - More complex pattern such as 00110011... (of length n_{sff}+4) may be necessary
    - To verify that all possible data transitions are possible
  - These tests are often called *flush tests*
- Test sequences for scan flip-flops based on checking experiments
  - Checking experiments are exhaustive tests for sequential circuits and detect all combinational faults

Total Scan Test

- Total scan test length:
  - $(n_{comb} + 2)\ n_{sff} + n_{comb} + 4$ *clock periods*.
- Example:
  - 2,000 scan flip-flops, 500 comb. vectors,
  - total scan test length ~ 10^6 clocks.
- Multiple scan registers reduce test length.

Issues

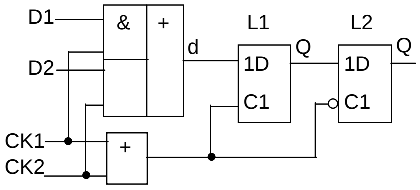
- The MD-flip-flop based scan path architecture does not need to route any extra clock
- However, the test signal T has to be routed to all flip-flop
  - Depending on the layout, the routing of the test signal T with proper skew control limits the speed at which scan shift can be done
    - Scan speeds between 10 MHz to 200 MHz aren’t uncommon
- Another factor that limits the speed at which the scan chains can be operated is the amount of power dissipation during scan

Two-port Flip-flop Architectures

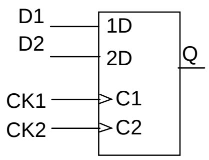
- Basic requirement of the scan path
  - Be able to gate data into the system flip-flops from two different sources
- Approaches
  - Add multiplexers to the system flip-flops: MD flip-flop
  - Replace each system flip-flop by a *two-port flip-flop*
    - A flip-flop having two control inputs with the data source determined by which of the control inputs is pulsed

Two-port Flip-flop Architectures

- Two-port flip-flop
  - When a pulse is applied to C1, data is entered from D1
  - When a pulse occurs at C2, data is entered from D2



(a)



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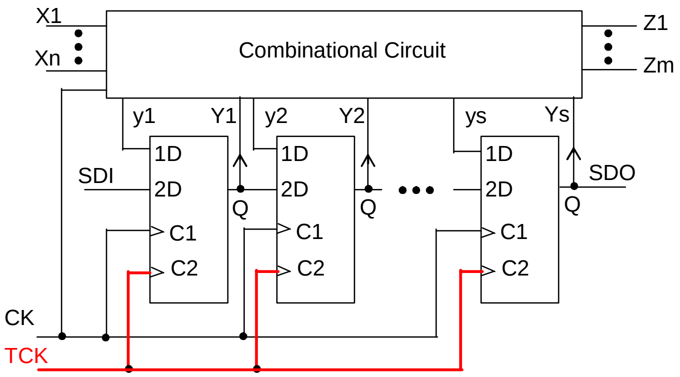
Two-port Flip-flop Scan Architecture

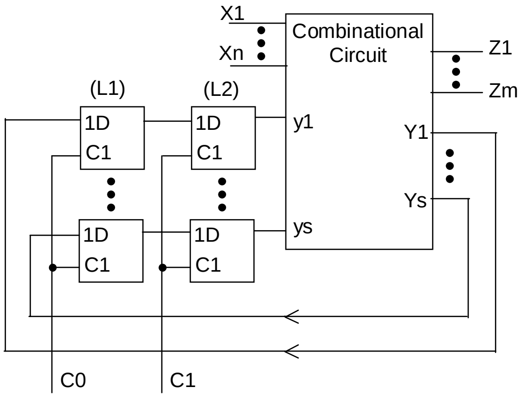


Modified Test Procedure

1. Scan in the test vector y_j values via Xn using test clock *TCK*
2. Set the corresponding test values on the X_i inputs.
3. After sufficient time for the signals to propagate through the combinational network, check the output Z_k values.
4. Apply one clock pulse to the system clock CK to enter the new values of Yj into the corresponding flip-flops.
5. Scan out and check the Yj values by pulsing test clock *TCK*

Two-Phase Latch Machines

- General structure of a two-phase double latch finite state machine

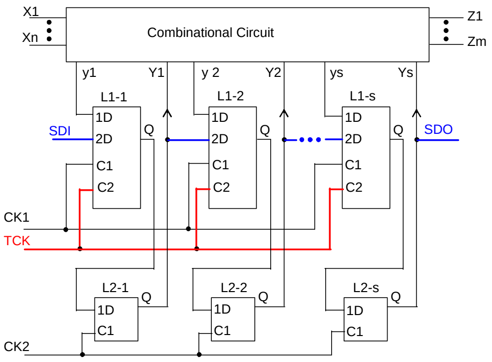


Two-Phase Latch Machines

- Edge-triggered D-flip-flops have been replaced by two latches in a master-slave connection
  - The master latches are called L1 latches,
    - Those with inputs from the combinational logic block
  - The slave latches are called L2 latches
    - Whose inputs come from the master latches
- A clock skew driver is used to derive the control signals CK1 and CK2 of the latches
  - CK1 and CK2 signals do not overlap
    - They are never both equal to 1 at the same time
  - This is to reduce various hazards in sequential circuits
    - Arise when clock and data inputs change at the same time
  - There can be an overlap between CK1 and CK2 to speed up circuit
    - Must be controlled: short path constraints are not violated

IBM's LSSD

- Level Sensitive Scan Design
  - Standard design technique in current use at IBM
  - L1 latch is replaced by a two-port (dual-port) latch



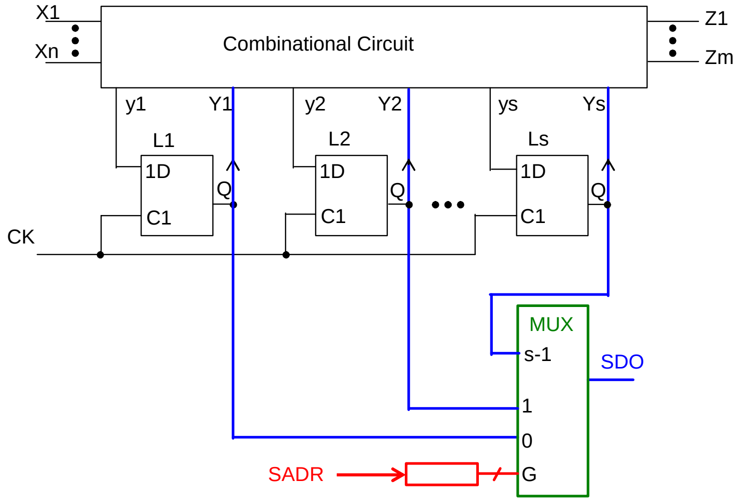
Test Application Procedure

1. Scan in the test vector y_j values via SDI by applying pulses alternately to the test clock input *TCK* and the system clock input CK2
2. Set the corresponding test values on the Xi inputs.
3. After sufficient time for the signals to propagate through the combinational network, check the output Zk values.
4. Apply one clock pulse to the system clock CK1 to enter the new values of y_j into the corresponding L1 latches.
5. Scan out and check the y_j values by applying clock pulses alternately to CK2 and *TCK*.

Multiplexer Scan Structures

- Parallel data can be serialized with a multiplexer rather than a shift register
- Use of more than one scan-out point increases the speed of scanning,
  - But does increase the number of I/O connections required.
  - One possibility for avoiding this increase is to place multiplexers on output pins to permit some of the output pins to be used both for system output and for scanning out test data
- With a multiplexer scan structure, nodes other than latch outputs can be accessed
  - The scanning operation can take place while the system is operating

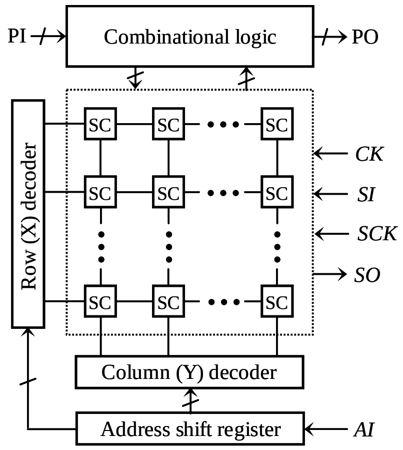
Multiplexer Scan Structures



Random Access Scan Design

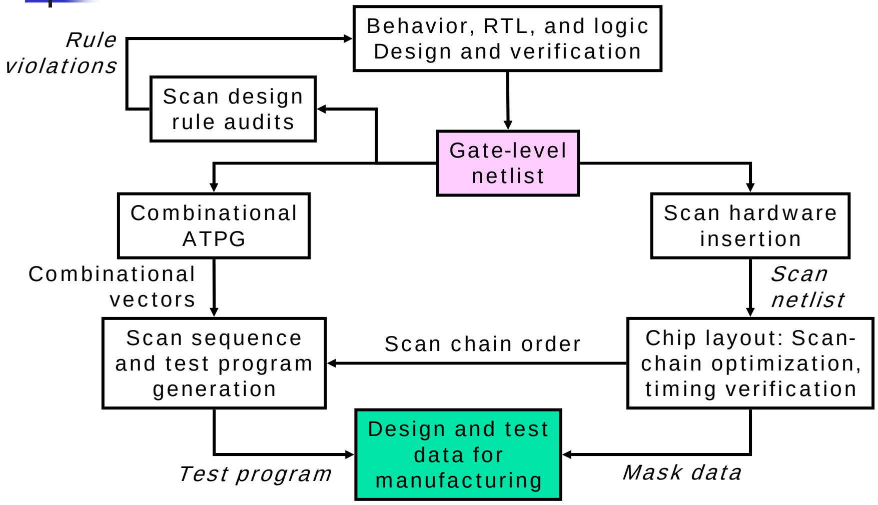
- Multiplexer structure improves the observability of a design
  - But does nothing for the controllability
  - Setting of the system latches can be accomplished with a demultiplexer
- Random access scan design
  - Multiplexer to read out bistables (observability)
  - Demultiplexer to set bistables (controllability)
    - Addressable latch

Traditional Random-Access Scan Architecture



All scan cells are organized into a two-dimensional array. A $\lceil \log_2^n \rceil$ -bit address shift register, where *n* is the total number of scan cells, is used to specify which scan cell to access.

Automated Scan Design



Scan Economics

- Additional circuitry is added to each flip-flop or latch
- One or more additional circuit pins are required
  - The number of additional pins required for scan test has a direct relationship with the test time
- Testing time is increased by the need to shift the test patterns into the flip-flops serially
  - The modified circuit requires shorter test sets than the original circuit
    - Because only combinational logic test patterns are used
- There can be a performance penalty.
  - The speed of normal operation may be decreased due to increased propagation delay in the scan path latches or flip-flops
- Available functional area can be reduced due to the increased interconnect
- Timing closure can be a problem
- Power dissipation during scan

Summary

- Scan is the most popular DFT technique:
  - Rule-based design
  - Automated DFT hardware insertion
  - Combinational ATPG
- Advantages:
  - Design automation
  - High fault coverage; helpful in diagnosis
  - Hierarchical – scan-testable modules are easily combined into large scan-testable systems
  - Moderate area (~10%) and speed (~5%) overheads
- Disadvantages:
  - Large test data volume and long test time
  - Basically a slow speed (DC) test