


Testing Digital Systems I

Lecture 1: Introduction

Instructor: M. Tahoori

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Today's Lecture

- Logistics
- Course Outline
- Introduction

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Logistics

- Instructor: Mehdi Tahoori
 - Office: Room B2-313.1, Building 07.21
 - Email: mehdi.tahoori@kit.edu
 - Tel: 721-608-47778, Fax: 721-608-43962
- Lecture:
 - When: Tuesdays 11:30-13:00
 - Where: Multimedia HS -101, Building 50.34



Logistics (cont)

- Requirements
 - Logic Design
 - Computer Architecture
- Background on (preferred but not required)
 - Algorithms and Programming
 - Hardware description languages (VHDL or Verilog)



Reference Books

- Textbook
 - **Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits** by M. L. Bushnell and V.D. Agrawal, *Kluwer Academic Press*, Boston 2000
- Recommended
 - **System On Chip Test Architectures: Nanometer Design for Testability** by L.T. Wang, C.E. Stroud, N. A. Touba, Elsevier, Morgan Kaufmann Publishers, 2009.
 - **Digital System Testing and Testable Design** by M. Abramovici, M. A. Breuer, and A.D. Friedman, *IEEE Press*, New York, 1990, 652 pages



Course Outline

- Basics
- Test generation methods
- Design for Testability (DFT)

- I try to be flexible. The order and contents may be changed as we proceed.



Outline: Basics

- Introduction
- Failures and errors
- Fault models
- Functional vs Structural testing



Outline: Test Generation

- Test generation techniques and algorithms for combinational logic
- Essentials of test generation methods for sequential circuits
- Logic and fault simulation

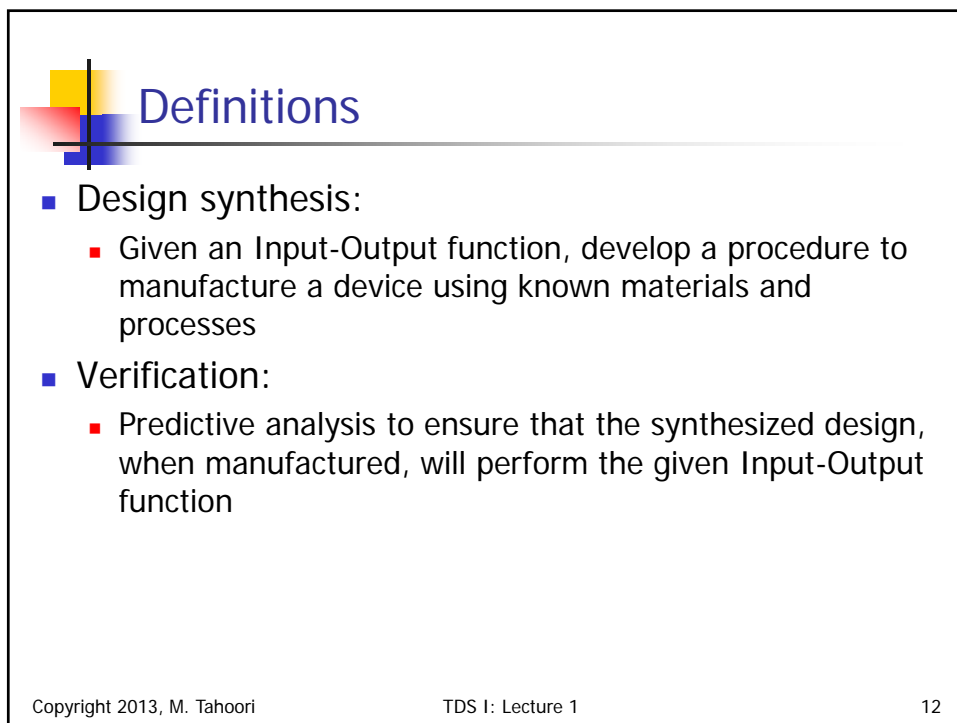
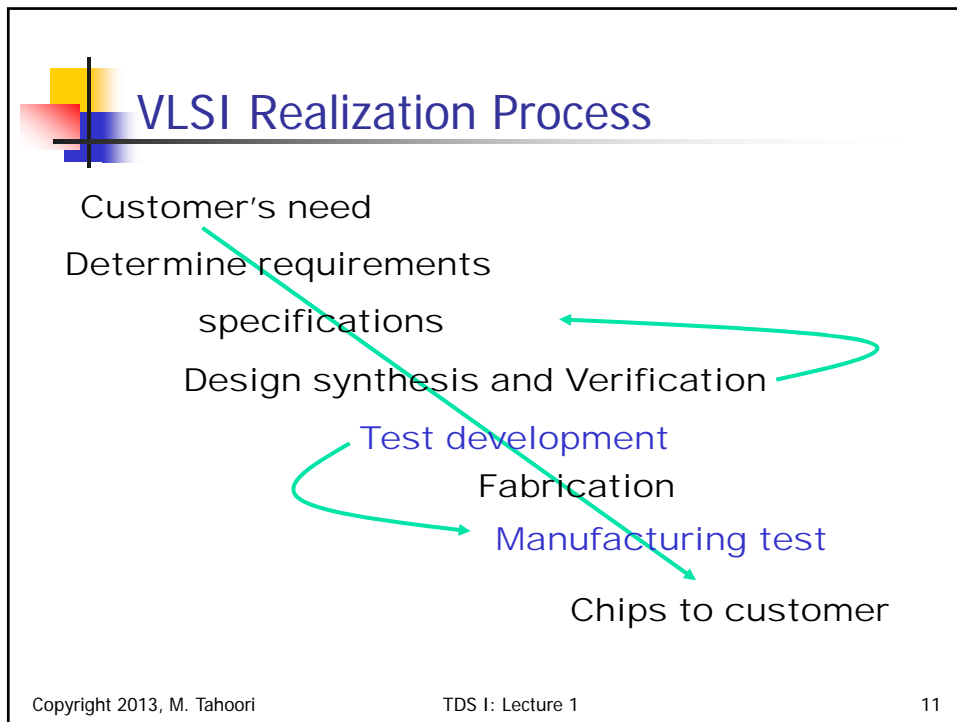


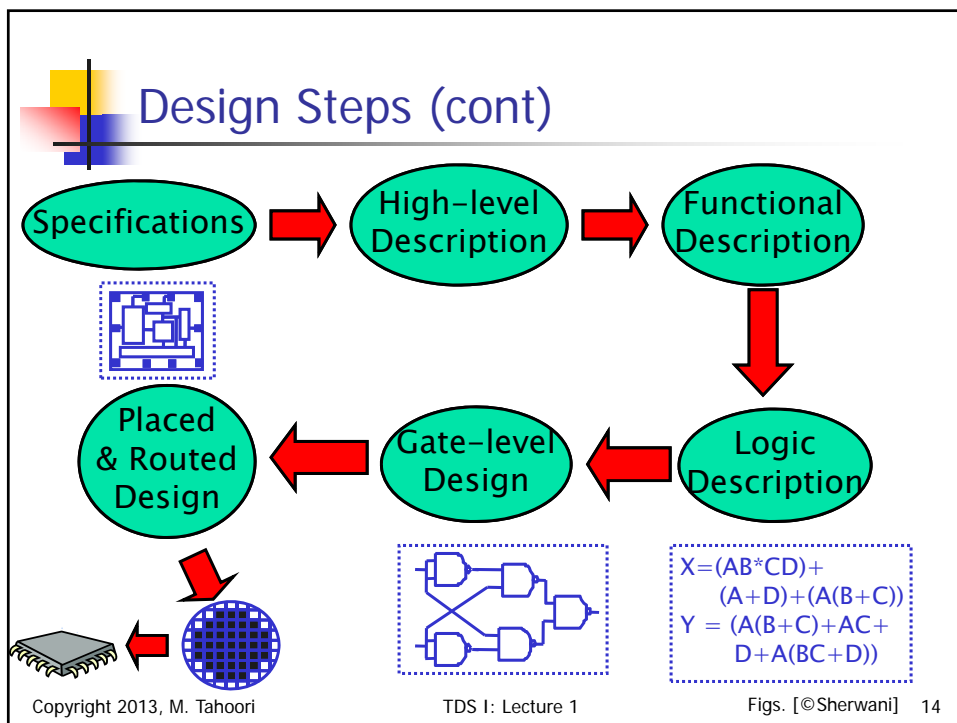
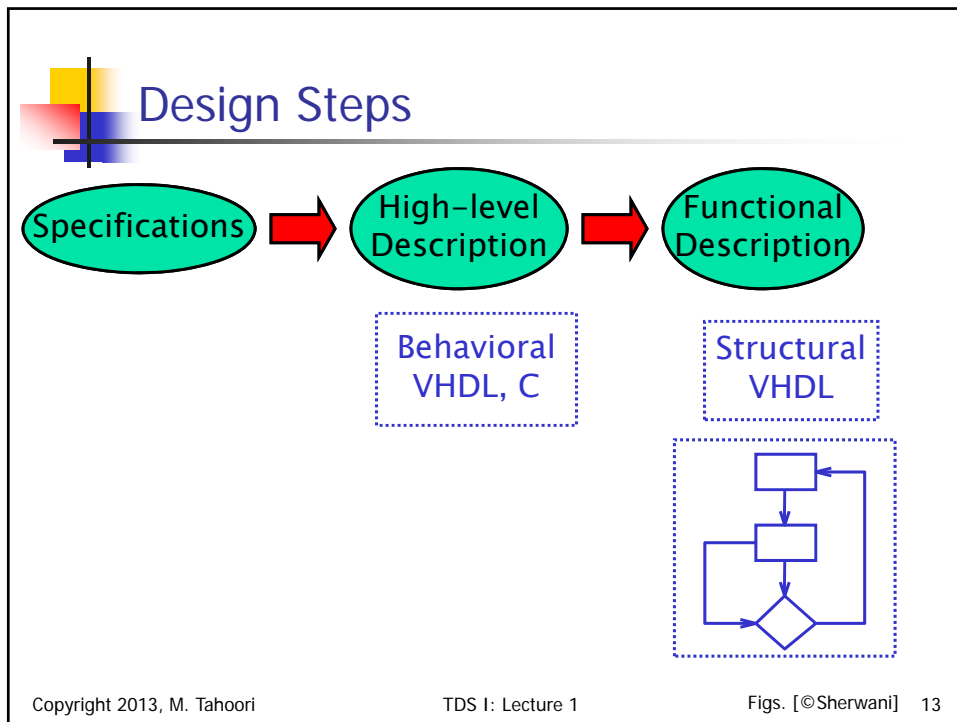
Outline: Design For Testability (DFT)

- Ad hoc DFT techniques
- Internal scan design
- Boundary scan



Introduction







Testing

- The process of determining whether a piece of device
 - Is functioning correctly, or
 - Is defective (broken or faulty)
- Equipment can be defective because it doesn't function
 - as designed, or
 - as specified



Testing (cont)

- The need for test depends on
 - Process yield, Y ,
 - the proportion of finished units that are not defective
 - Depends on maturity of the manufacturing process, size of the integrated circuit chips and the characteristics of the implemented design, etc.
 - Acceptable quality level (AQL)
 - the planned minimum fraction of defective shipped units
 - Defective Parts per Million (DPM)
 - Depends on the volume of the product, criticality of the applications and the cost of the parts

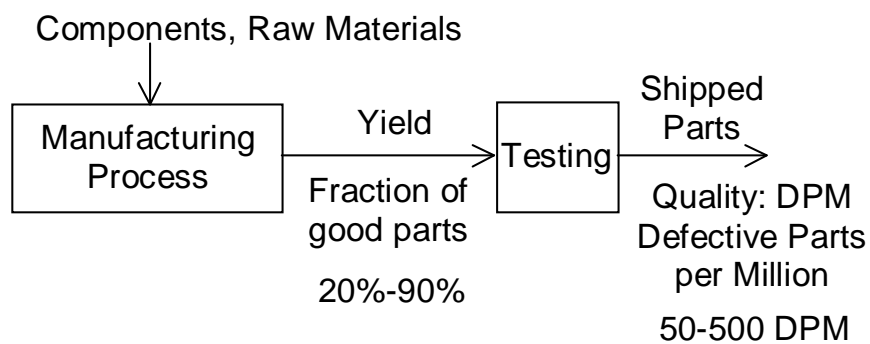


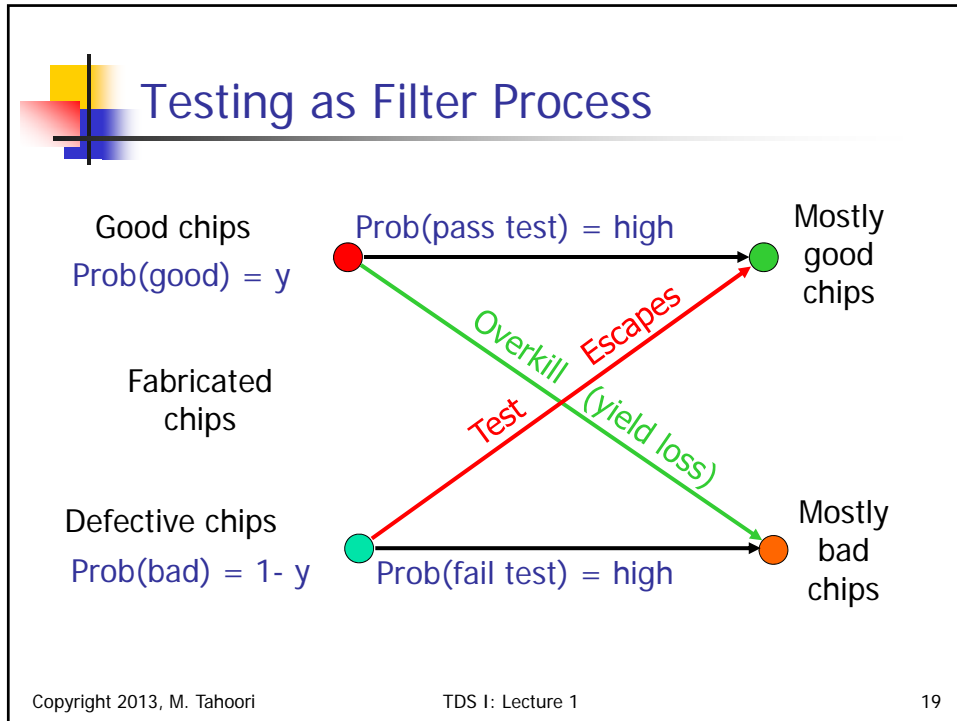
Yield and Quality Level

- Y and AQL are rarely exactly known
 - Statistically estimated
 - Not feasible to thoroughly test all parts
- Process yield is typically less than AQL
 - defective units must be identified and removed so as to increase the percentage of good units shipped to the customer.



Testing Process







Logic Design Verification

- Specification
 - Behavioral or Register Transfer
 - Table of Combinations – Boolean Function
 - Sequential Circuit or State Machine Flow Table
 - Simulation Vectors and Responses
 - Informal Word Description of Functionality
- Verification Technique
 - Synthesis
 - Matching of Two Design Paths
 - Simulation — Emulation
 - Formal Verification



Verification vs. Test

- | | |
|---|---|
| <ul style="list-style-type: none">■ Verifies correctness of design.■ Performed by simulation, hardware emulation, or formal methods.■ Performed once prior to manufacturing.■ Responsible for quality of design. | <ul style="list-style-type: none">■ Verifies correctness of manufactured hardware.■ Two-part process:<ul style="list-style-type: none">■ 1. Test generation: software process executed once during design■ 2. Test application: electrical tests applied to hardware■ Test application performed on every manufactured device.■ Responsible for quality of devices. |
|---|---|



Problems of Ideal Tests

- Definition
 - Ideal tests detect all defects produced in the manufacturing process.
 - Ideal tests pass all functionally good devices.
- Problems
 - Very large numbers and varieties of possible defects need to be tested.
 - Difficult to generate tests for some real defects.
 - Unacceptable test costs
 - Test generation effort, test application time



Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected
 - The fraction (or percentage) of such chips is called the *yield loss*.
- Some bad chips pass tests
 - The fraction (or percentage) of bad chips among all passing chips is called the *defect level*.



VLSI Technology an Trends

- These trends impact cost and difficulty of testing

Year	97-01	03-06	09-12
Feature size (um)	0.25-0.15	0.13-0.10	0.07-0.05
Millions of transistors/cm ²	4-10	18-39	84-180
Number of wiring layers	6-7	7-8	8-9
Die size, mm ²	50-385	60-520	70-750
Pin count	100-900	160-1475	260-2690
Clock rate, MHz	200-730	530-1100	840-1830
Voltage, V	1.2-2.5	0.9-1.5	0.5-0.9
Power, W	1.2-61	2-96	2.8-109

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Costs of Testing

- *Design for testability* (DFT)
 - Chip area overhead
 - Yield reduction
 - Performance overhead
- Software processes of test
 - Test generation
 - Fault simulation
 - Test programming and debugging
- Manufacturing test
 - *Automatic test equipment* (ATE) capital cost
 - Test center operational cost

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Example: Cost of Testing

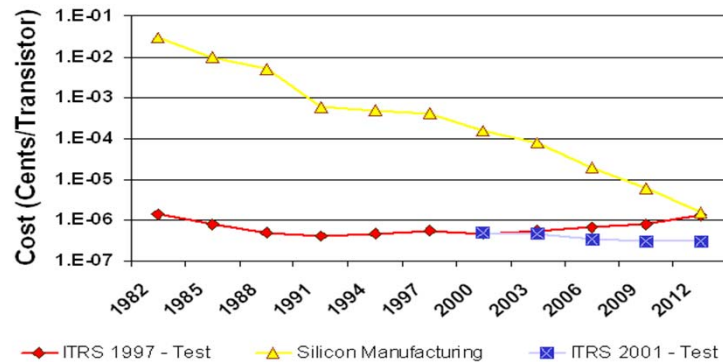
- 0.5-1.0GHz, analog instruments, 1,024 digital pins:
ATE purchase price
 - = $\$1.2\text{M} + 1,024 \times \$3,000 = \$4.272\text{M}$
- Running cost (five-year linear depreciation)
 - = Depreciation + Maintenance + Operation
 - = $\$0.854\text{M} + \$0.085\text{M} + \$0.5\text{M}$
 - = $\$1.439\text{M}/\text{year}$
- Test cost (24 hour ATE operation)
 - = $\$1.439\text{M}/(365 \times 24 \times 3,600)$
 - = 4.5 cents/second
- Digital ASIC test time: 6 seconds or 27 cents

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Cost of Manufacturing Test



Source: International Technology Roadmap for Semiconductor Industry (ITRS)

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Roles of Testing

- Detection:
 - Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis:
 - Identification of a specific fault that is present on DUT.
- Device characterization:
 - Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA):
 - Determination of manufacturing process errors that may have caused defects on the DUT.



Who Needs to Take This Class?

- Testing (Test & DFT Engineer)
 - Needs to focus on all topics,
 - More emphasize on test flow and tools
- Design automation (CAD Engineer)
 - Focus on test generation and DFT algorithms
 - Test automation
- Circuit design and computer architecture (Designer)
 - Focus on DFT techniques
 - Testable designs
 - Interaction of test flow and design flow
 - How DFT affect the original design