


# Testing Digital Systems I

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## Lecture 8: Boolean Testing Using Fault Models (D Algorithm)

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## Specific-Fault Oriented Test Generation

- Three Approaches
  - Internal Line Values Assigned ( D Algorithm) (Roth-1966)
    - D-cubes
    - Bridging faults
    - Logic gate function change faults
  - Input Values Assigned (PODEM) (Goel – 1981)
    - X-Path-Check
      - Path propagation constraints to limit ATPG search space
    - Backtracing
  - Input and Internal Values Assigned (FAN) (Fujiwara)
    - Efficiently constrained backtarce

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## Fault Cone and D-frontier

- Fault Cone
  - Set of hardware affected by fault
- D-frontier
  - Set of gates closest to POs with fault effect(s) at input(s)

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## D Algorithm

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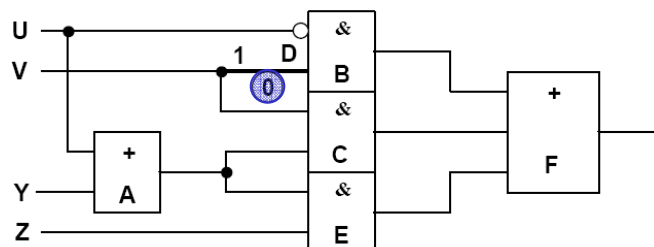
## D-Algorithm -- Roth IBM (1966)

- Fundamental concepts invented:
  - First complete ATPG algorithm
  - D-Cube
  - D-Calculus
  - Implications – forward and backward
  - Implication stack
  - Backtrack
  - Test Search Space



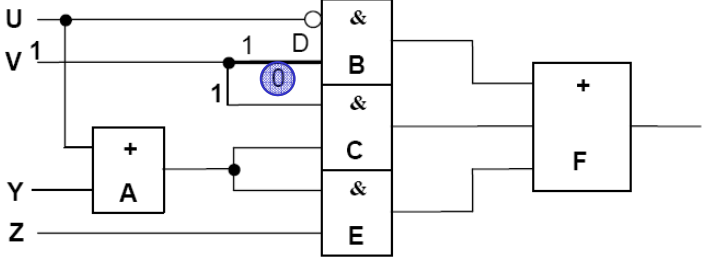
## D Algorithm

- Assigning internal line values
- Example:
  - Test for Stuck-at-0 on Lower Input to Gate B
  - Activate Fault — Put 1 on Faulty Lead



## D Algorithm

- Example
  - Test for Stuck-at-0 on Lower Input to Gate B
- Implication
  - Record Effects of Previous Assignments

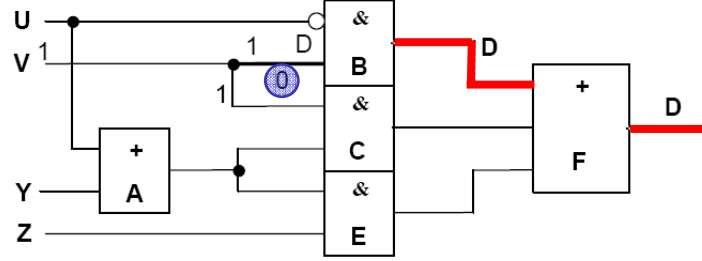


The diagram shows a digital circuit with inputs U, V, Y, and Z. Gate A is an adder (+) with inputs Y and Z. Gate B is an AND (&) gate with inputs U and V. Gate C is an AND (&) gate with inputs V and the output of Gate A. Gate E is an AND (&) gate with inputs U and the output of Gate A. Gate F is an adder (+) with inputs from Gate B and Gate C. A 'D' symbol is placed on the lower input of Gate B, with a '1' on the line leading to it, indicating a stuck-at-0 fault. A '1' is also shown on the line from V to Gate C.

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## D Algorithm

- Propagation
  - Select Path to Propagate D to Output
  - Single versus Multiple Path Propagation



This diagram is identical to the one in slide 7, but it highlights the propagation of the 'D' fault. A red line starts from the 'D' symbol on the lower input of Gate B, passes through Gate B, and then enters Gate F from its top input. The output of Gate F is also marked with a red line and the letter 'D', showing that the fault has propagated to the final output.

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## D Algorithm

- Propagation
  - Assign Required Gate Input Values
  - 0s on other inputs of OR, NOR Gates with D or  $\bar{D}$  Input
  - 1s on other inputs of AND, NAND Gates with D or  $\bar{D}$  Input

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## Line Justification

- Find Input Assignment to Place Value v on Line g
- Path Tracing Approach
  - Propagate Signals using Element Functions
  - Must Choose Element Input Values and Paths
- Primitive cube of an element (gate) with output Z
  - List of prime implicants of Z and Z'

AND		
A	B	Z
1	1	1
0	—	0
—	0	0

NAND		
A	B	Z
1	1	0
0	—	1
—	0	1

Implication (no choices)

Decision (choices)

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## D Algorithm

- Line Justification
  - Assign Required Gate Input Values
  - 0 on lower input of C to give 0 on output

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## D Algorithm

- Implication
  - Record Effects of Previous Assignments
- Test is  $U, V, Y, Z = 0, 1, 0, d$
- DIFFICULTY
  - Internal Line Values May be Inconsistent

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## D Algorithm

- Example
  - Test for Stuck-at-1 on Gate A Output
- Activate Fault
  - Put 0 on Faulty Lead

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## D Algorithm

- Example
  - Test for Stuck-at-1 on Gate A Output
- Implication
  - Record Effects of Previous Assignments

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## D Algorithm

- Example
  - Test for Stuck-at-1 on Gate A Output
- Propagation
  - Select Path to Propagate D to Output

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## D Algorithm

- Propagation
  - Assign Required Gate Input Values
  - 0s on other inputs of OR, NOR Gates with D or  $\bar{D}$  Input
  - 1s on other inputs of AND, NAND Gates with D or  $\bar{D}$  Input

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### D Algorithm

- Example
  - Test for Stuck-at-1 on Gate A Output
- Implication
  - Record Effects of Previous Assignments

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### D Algorithm

- Example
  - Test for Stuck-at-1 on Gate A Output
- Propagation
  - Select Alternate Path to Propagate D to Output

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## D Algorithm

- Example
  - Test for Stuck-at-1 on Gate A Output
- Implication
  - Record Effects of Previous Assignments
- Test is  $U, V, Y, Z = 0, 0, 0, 1$

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## D Calculus

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## Singular Cover

- Singular Cover
  - Minimal set of input signal assignments to show essential prime implicants of Karnaugh map

Gate	Inputs	Output	Gate	Inputs	Output
AND	A B	d	NOR	d C	F
1	0 X	0	1	1 X	0
2	X 0	0	2	X 1	0
3	1 1	1	3	0 0	1


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## D Algorithm

- D-Cube
  - A collapsed truth table entry
- Example
  - AND gate

	A	B	d
Rows 1 & 3	D	1	D
Reverse inputs	1	D	D
And two cubes	<u>D</u>	<u>D</u>	<u>D</u>
Interchange D and <u>D</u>	<u>D</u>	<u>D</u>	<u>D</u>
	1	D	<u>D</u>
	<u>D</u>	1	<u>D</u>

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## D Algorithm

- D Intersection
  - Defines how different D-cubes can coexist for different gates in logic circuit
  - If one cube assigns a specific signal value, the other cubes must assign either that same value or X
  - $1 \cap 1 = 1 \cap X = X \cap 1 = 1$
  - $0 \cap 0 = 0 \cap X = X \cap 0 = 0$
  - $X \cap X = X$

$\psi, \phi$  represent incompatible assignments  
 $\mu, \lambda$  represent incompatibility if both present

$\cap$	0	1	X	D	$\bar{D}$
0	0	$\phi$	0	$\psi$	$\psi$
1	$\phi$	1	1	$\psi$	$\psi$
X	0	1	X	D	$\bar{D}$
$\bar{D}$	$\psi$	$\psi$	$\bar{D}$	$\mu$	$\lambda$
D	$\psi$	$\psi$	D	$\lambda$	$\mu$

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## D Algorithm

- Primitive D-cube of Failure (PDF)
  - Models fault including
    - SA1: represented by  $\bar{D}$
    - SA0: represented by D
  - Example: AND gate
    - PDF for output SA0 is 1 1 D
    - PDFs for output SA1 are 0 X  $\bar{D}$ , X 0  $\bar{D}$
- Propagation D-cube
  - Models conditions under which fault effect propagates through gate

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## Implication Procedure

1. Model fault with appropriate PDF
2. Select propagation D-cubes to propagate fault effect to a PO (**D-drive** procedure)
3. Select singular cover cubes to justify internal circuit signals (**Consistency** procedure)

- D Algorithm's main problem
  - Selects cubes and singular covers arbitrarily

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