Testing Digital Systems I

Lecture 3:

Quality Models and Yield Analysis

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VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol *Y*.
- Cost of a chip:

$$\frac{\text{Cost of fabricating and testing a wafer}}{\text{Yield x Number of chip sites on the wafer}}$$

Definitions

- Quality Level, QL
  - Fraction of Parts Passing Test that are Good
- Defect Level, DL = 1 - QL
  - Fraction of Parts Passing Test that are ~~Good~~ BAD
    - Measured in DPM, Defects per Million
    - Typical Claim is Less than 200 DPM (0.02 %)
- Yield, Y
  - Fraction of Manufactured Parts that are Good
    - Typically 10 to 90 %
- Reject Ratio
  - Fraction of Manufactured Parts that Fail Test
    - Used to Estimate Yield

Determination of DL

- From field return data:
  - Chips failing in the field are returned to the manufacturer.
  - The number of returned chips normalized to one million chips shipped is the DL.
- From test data:
  - Fault coverage of tests and chip fallout rate are analyzed.
  - A modified yield model is fitted to the fallout data to estimate the DL.

Test Thoroughness

- Measured by
  - Test transparency, TT
    - Fraction of Defects NOT Detected by Test
    - Estimated by FAULTS Missed by Test
      - Faults are Logical Models of Defects
- Required Test Transparency
  - Depends on Yield and Acceptable Quality Level

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Estimating Board Quality Level

- N Components per Board
- Component Defects are Identical and Independent
- Each Component has Probability, q, of being Defective
- Probability that Board has no Defective Component is:
  - $P = (1 - q)^N$

N	DL	q	P %	1-P
40	10,000 DPM	10^{-2} or 1 %	66.9	33.1
200	10,000 DPM	10^{-2} or 1 %	13.4	86.6
40	1000 DPM	10^{-3} or 0.1 %	96	4
200	1000 DPM	10^{-3} or 0.1 %	82	18
40	100 DPM	10^{-4} or 0.01 %	99.6	0.4
200	100 DPM	10^{-4} or 0.01 %	98	2

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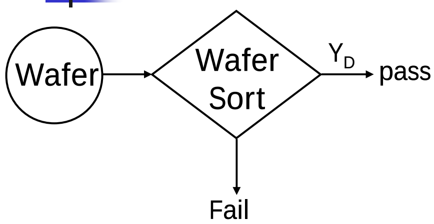
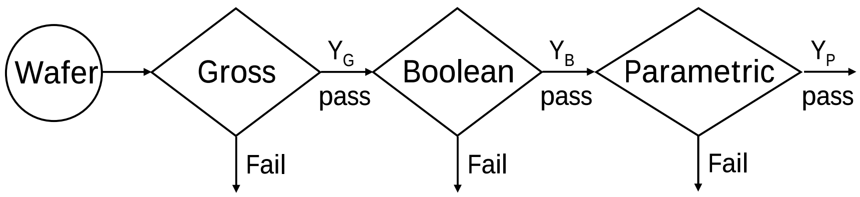
Wafer Sort (Wafer Probe,Probe Test)



- Y, Yield = Fraction of die passing test
- Y_D = Die Yield
- Y_G = Gross Yield
- Y_B = Boolean Yield
- Y_P = Parametric Yield



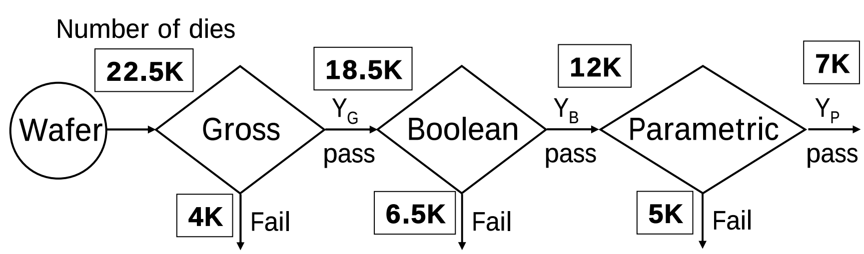
Wafer Sort

- Gross Test
  - Test for Gross Defects - Idd, Pin Leakage,...
- Parametric Test
  - Measure analog parameters of device
    - DC - Voltage levels, drive current, power,...
    - AC - Rise, fall, delay times
- Boolean Test
  - Digital test of Logic Operation
  - Called Functional Test by Chip Testers
  - Based on Fault Model

Wafer Sort Definitions

- Die yield, Y_D,
  - Fraction of Die that are defect-free
  - *ESTIMATED* by Fraction of Die that pass Wafer Sort
- Boolean (functional) defect
  - Defect that Changes Function Realized by Die
- Boolean (functional) Yield, Y_B,
  - Fraction of Die that are free of Boolean defects
  - *ESTIMATED* by Fraction of Die that Pass Boolean Test
- Boolean (functional) test
  - Test for Boolean (functional) Defects

Motorola6802 Wafer Sort Experiment



- Single Stuck-Fault Coverage = 99.9 %
- Y_B = 12 /18.5 = 65.167 %
- Y_G = 18.5 / 22.5= 82.2 %
- Y_P= 7 / 12.00= 58 %

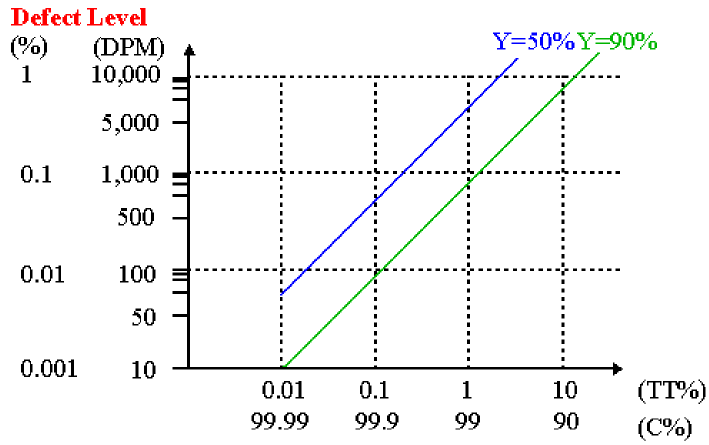
What If

- Single stuck-fault coverage were 96.6 % ?
  - Theory Predicts:
    - DL = 14,454 DPM or 174 Bad Die Pass Boolean Test
  - Experiment shows:
    - DL = 8,471 DPM or 103 Bad Die Pass Boolean Test

Quality Level Dependence On Y & TT

- Theorem:
  - The Boolean Quality Level achieved by a test with Boolean Test Transparency, TT, for a process of Boolean Yield, Y, is given by:
    - $QL = Y^{TT}$
- Corollary:
  - For Tests that Result in Defect Levels, DL, less than 1000 DPM this can be simplified to:
    - DL = (-ln Y) TT
  - And further simplified for Y $\geq$ 90 % to:
    - DL = (1 -Y) TT

Relationship Between DL and TT



Derivation Of Theorem (1)

- n Possible Point Defects on Chip
- **Assumption:** defects are independent and equally distributed
- m of the n Defects Detected by Test Set, (n - m) Not Detected
- TT is (n - m)/n = 1 – (m / n)
- p is Probability of a Defect Occurring
- A is Event that Die has no Defects
  - Yield $Y = P[A] = (1 - p)^n$
- B is event that die passes test, none of the m defects on die
  - $P[B] = (1 - p)^m$
  - if a chip is free of defects, it is free of m tested defects
    - $P[AB] = P[A] = (1 - p)^n$

Derivation Of Theorem (2)

- QL is given by the probability that a chip is free of all *n* defects when it is known that it is free of any of the *m* defects detected by the test process
- $QL = \dfrac{\text{Number of defect-free parts that pass the test}}{\text{Total number of parts that pass the test}}$
- QL = P[A|B] = P[AB]/P[B] = P[A]/P[B]
- $= (1 - p)^{(n - m)} = (1 - p)^{n(1 - m/n)} = Y^{TT}$

Simplifications (1)

- DL less than 1,000 DPM
  - $DL < 10^{-3} \Rightarrow QL = 1 – DL = Y^{TT} > 0.999$
  - $|TT \ln Y| < | \ln (0.999) | = 10^{-3}$
  - Series expansion of $QL = Y^{TT}$
    - $QL = Y^{TT} = 1 + TT \ln Y + (TT \ln Y)^2 / 2 + (TT \ln Y)^3 / 3! + ...$
  - Since $|TT \ln Y| < 10^{-3}$
    - $| (TT \ln Y)^2 / 2 + (TT \ln Y)^3 / 3! + ...| < 10^{-6}$
  - $QL \approx 1 + TT \ln Y$
  - $DL \approx TT (– \ln Y)$
  - $TT \approx – DL/(\ln Y)$

Simplifications (2)

- DL less than 1,000 DPM and Y = 90 %
  - $\ln Y = (Y - 1) - (Y - 1)^2 / 2 + (Y - 1)^3 / 3 - \ldots$
  - $-\ln Y = (1 - Y) + (1 - Y)^2 / 2 + (1 - Y)^3 / 3 + \ldots$
- $Y = 90\ \% \Rightarrow$
  - $(1 - Y) < 0.1$ and
  - $| 1 / 2 (1 - Y)^2 + 1 / 3 (1 - Y)^3 - \ldots | < 10^{-2}$

  - $(1 - Y) < (-\ln Y) < (1 - Y) + 10^{-2}$

$DL \approx TT(-\ln Y) \approx TT(1 - Y)$

Example

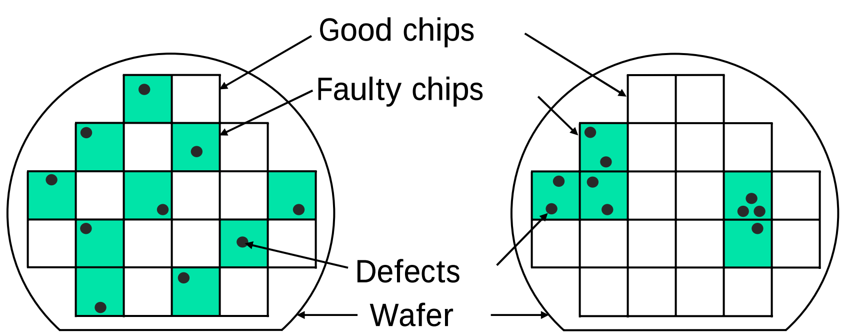
- Required TT and coverage (C) for DL=200 DPM

Y%	**10**	**50**	**75**	**90**	**95**	**99**
-ln Y	2.3	0.69	0.288	0.105	0.05	0.01
1/(-ln Y)	0.434	1.44	3.48	9.49	19.5	99.5
TT%	0.008	0.03	0.07	0.2	0.4	2
C%	99.992	99.97	99.93	99.8	99.6	98

Clustered Defects

Clustered VLSI Defects

- Clustering which happens in reality gives higher yield



Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Clustering Effect

- Cluster THEOREM:
  - The Boolean Quality Level achieved by a test
    - with Fault Coverage C,
    - for a process of Boolean Yield, Y
- $$QL = \frac{(1 - C)(1 - Y)e^{-(n-1)C}}{Y + (1 - C)(1 - Y)e^{-(n-1)C}}$$
- where n is average number of faults on a faulty die

What If (Motorola6802 Experiment)

- Single stuck-fault coverage were 96.6 % ?
  - Uniform Theory Predicts:
    - DL = 14,454 DPM or 174 Bad Die Pass Boolean Test
  - Cluster Theory with n=1 Predicts:
    - DL = 17,849 DPM or 217 Bad Die Pass Boolean Test
  - Cluster Theory with n=2 Predicts:
    - DL = 6,869 DPM or 84 Bad Die Pass Boolean Test
  - Experiment shows:
    - DL = 8,471 DPM or 103 Bad Die Pass Boolean Test

Yield Parameters

- Defect density (d)
  - Average number of defects per unit of chip area
- Chip area (A)
- Clustering parameter (α)
- Negative binomial distribution of defects,

$\boldsymbol{p}(x)$ = Prob (number of defects on a chip = x)

$$= \frac{\Gamma(\alpha+x)}{x!\,\Gamma(\alpha)} \cdot \frac{(Ad/\alpha)^{x}}{(1+Ad/\alpha)^{\alpha+x}}$$

where Γ is the gamma function

$\alpha = 0$, $p(x)$ is a delta function (max. clustering)

$\alpha = \infty$, $p(x)$ is Poisson distr. (no clustering)

Yield Equation

Y = Prob (zero defect on a chip) = $p(0)$

$$Y = (1 + Ad/\alpha)^{-\alpha}$$

Example: $Ad = 1.0$, $\alpha = 0.5$, $Y = 0.58$

Unclustered defects: $\alpha = \infty$, $Y = e^{-Ad}$

Example: $Ad = 1.0$, $\alpha = \infty$, $Y = 0.37$

too pessimistic **!**

Modified Yield Equation

- Three parameters:
  - Fault density, f
    - Average number of stuck-at faults per unit chip area
  - Fault clustering parameter, β
  - Stuck-at fault coverage, T
- The modified yield equation:

$$Y(T) = (1 + TAf / \beta)^{-\beta}$$

Assuming that tests with 100% fault coverage (T =1.0) remove all faulty chips,

$$Y = Y(1) = (1 + Af / \beta)^{-\beta}$$

Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

- T is the fault coverage of tests,
- Af is the average number of faults on the chip of area A
- β is the fault clustering parameter
- Af and β are determined by test data analysis.

Summary

- VLSI yield depends on two process parameters,
  - Defect density (*d*)
  - Clustering parameter (α)
- Yield drops as chip area increases
  - low yield means high cost
- Fault coverage measures the test quality
- Defect level (DL) or reject ratio is a measure of chip quality
- DL can be determined by an analysis of test data
- For high quality: DL < 500 DPM,
  - Fault coverage should be ~ 99%

