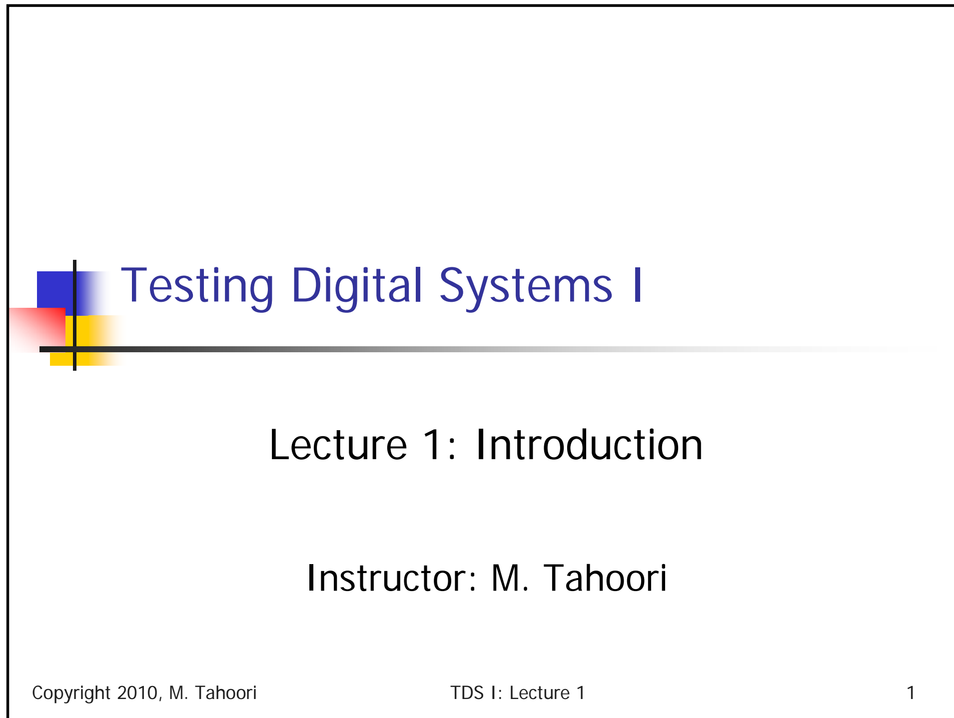
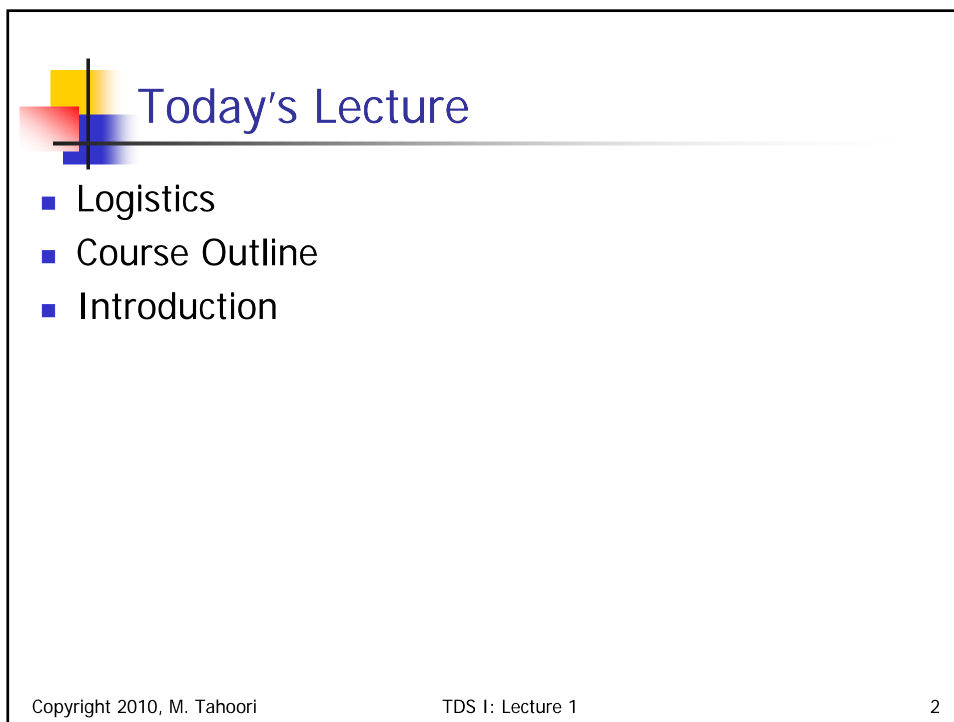
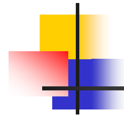
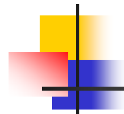

Testing Digital Systems I
Lecture 1: Introduction
Instructor: M. Tahoori
Copyright 2010, M. Tahoori
TDS I: Lecture 1
1


Today's Lecture
Logistics
Course Outline
Introduction
Copyright 2010, M. Tahoori
TDS I: Lecture 1
2



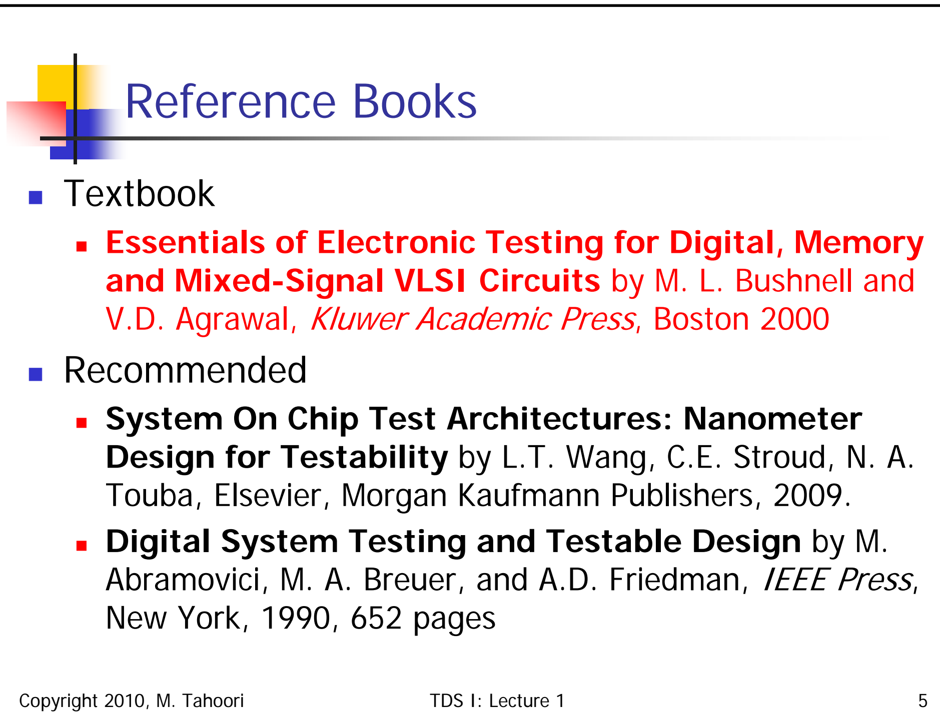
Logistics

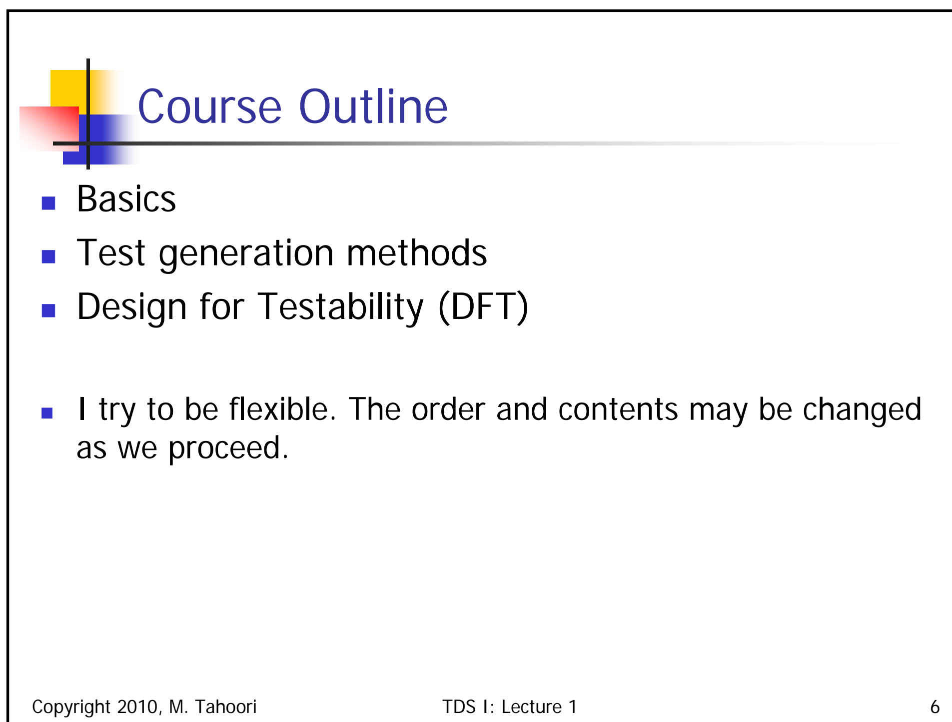
- Instructor: Mehdi Tahoori
  - Office: Room B2-313.1, Building 07.21
  - Email: mehdi.tahoori@kit.edu
  - Tel: 721-608-7778, Fax: 721-608-3962
- Lecture:
  - When: Thursdays 15:45-17:15
  - Where: Multimedia HS -101, Building 50.34

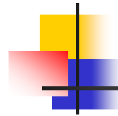


Logistics (cont)

- Requirements
  - Logic Design
  - Computer Architecture
  - Background on
    - Algorithms and Programming
    - Hardware description languages (VHDL or Verilog)

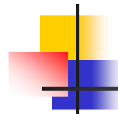

Reference Books
Textbook
Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. L. Bushnell and V.D. Agrawal, Kluwer Academic Press, Boston 2000
Recommended
System On Chip Test Architectures: Nanometer Design for Testability by L.T. Wang, C.E. Stroud, N. A. Touba, Elsevier, Morgan Kaufmann Publishers, 2009.
Digital System Testing and Testable Design by M. Abramovici, M. A. Breuer, and A.D. Friedman, IEEE Press, New York, 1990, 652 pages
Copyright 2010, M. Tahoori
TDS I: Lecture 1
5


Course Outline
Basics
Test generation methods
Design for Testability (DFT)
I try to be flexible. The order and contents may be changed as we proceed.
Copyright 2010, M. Tahoori
TDS I: Lecture 1
6



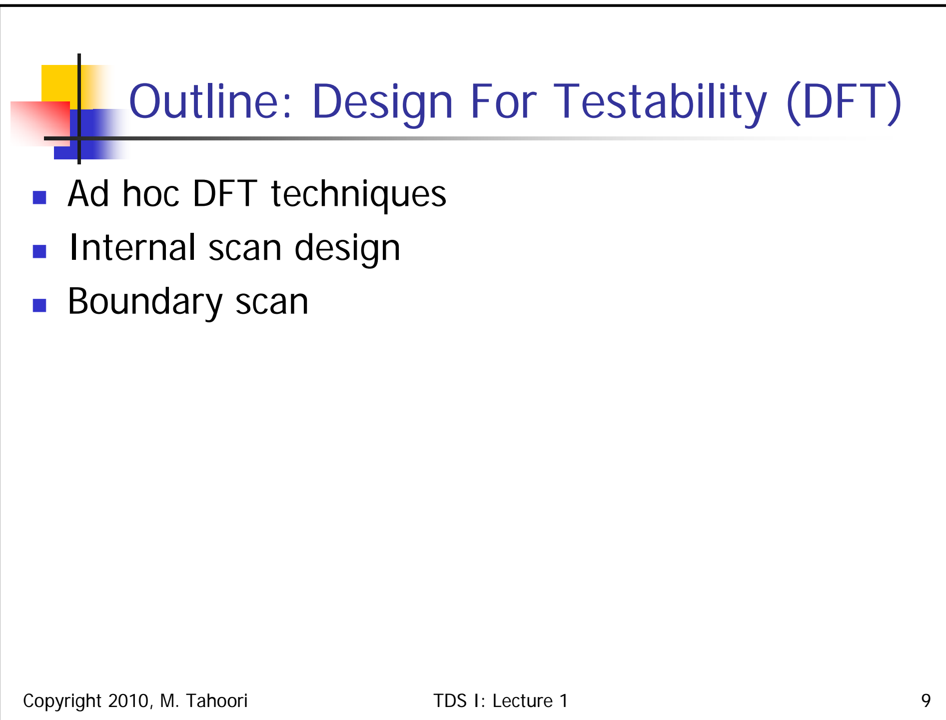
Outline: Basics

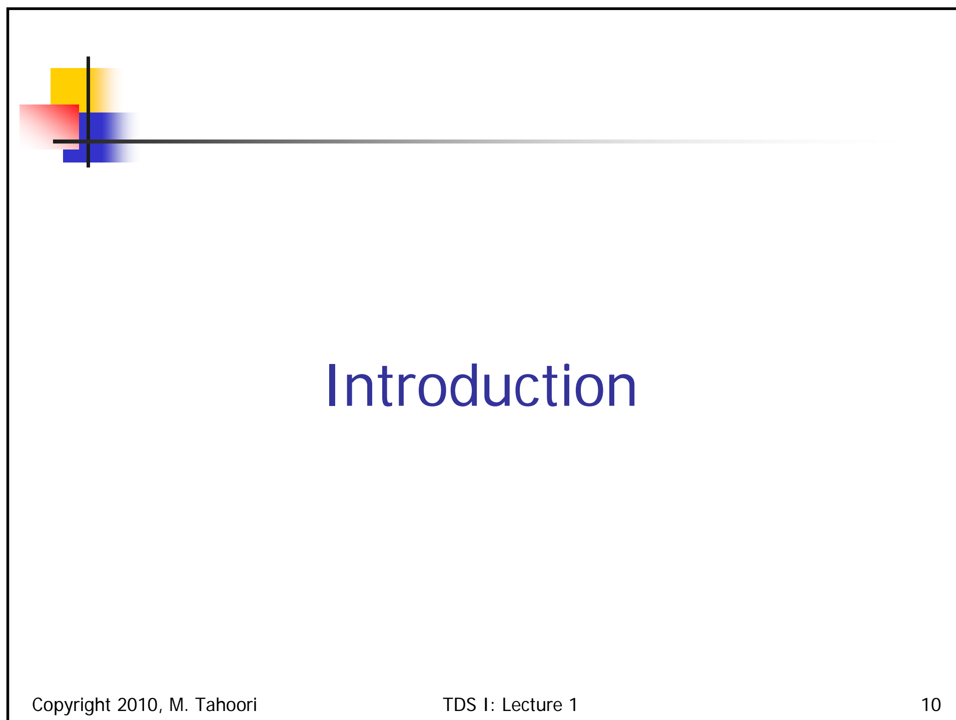
- Introduction
- Failures and errors
- Fault models
- Functional vs Structural testing

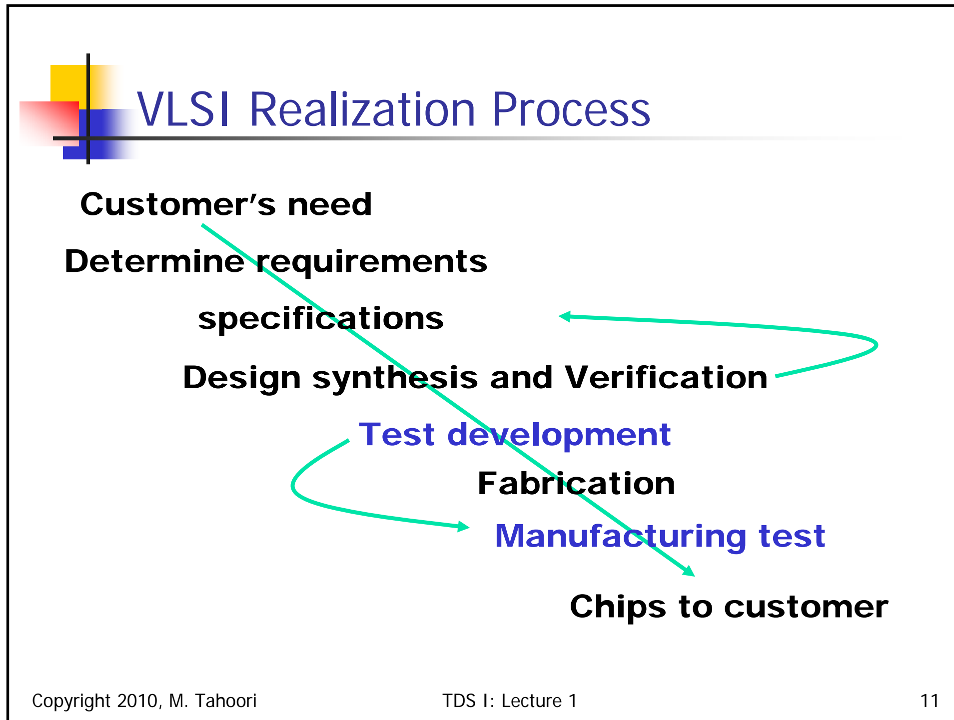


Outline: Test Generation

- Test generation techniques and algorithms for combinational logic
- Essentials of test generation methods for sequential circuits
- Logic and fault simulation


Outline: Design For Testability (DFT)
Ad hoc DFT techniques
Internal scan design
Boundary scan
Copyright 2010, M. Tahoori
TDS I: Lecture 1
9

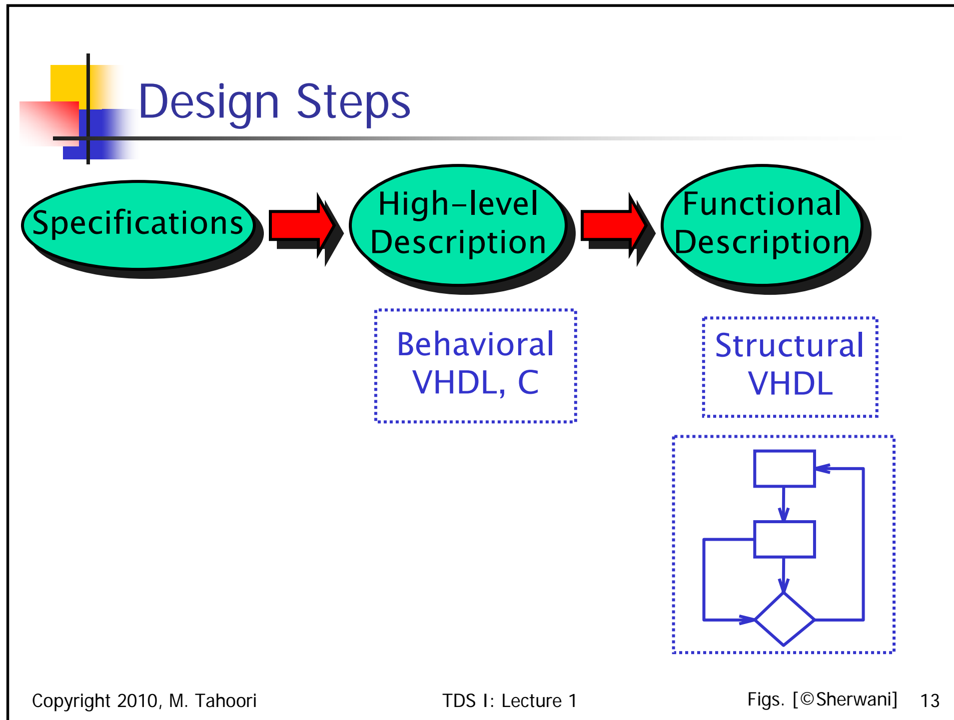

Introduction
Copyright 2010, M. Tahoori
TDS I: Lecture 1
10

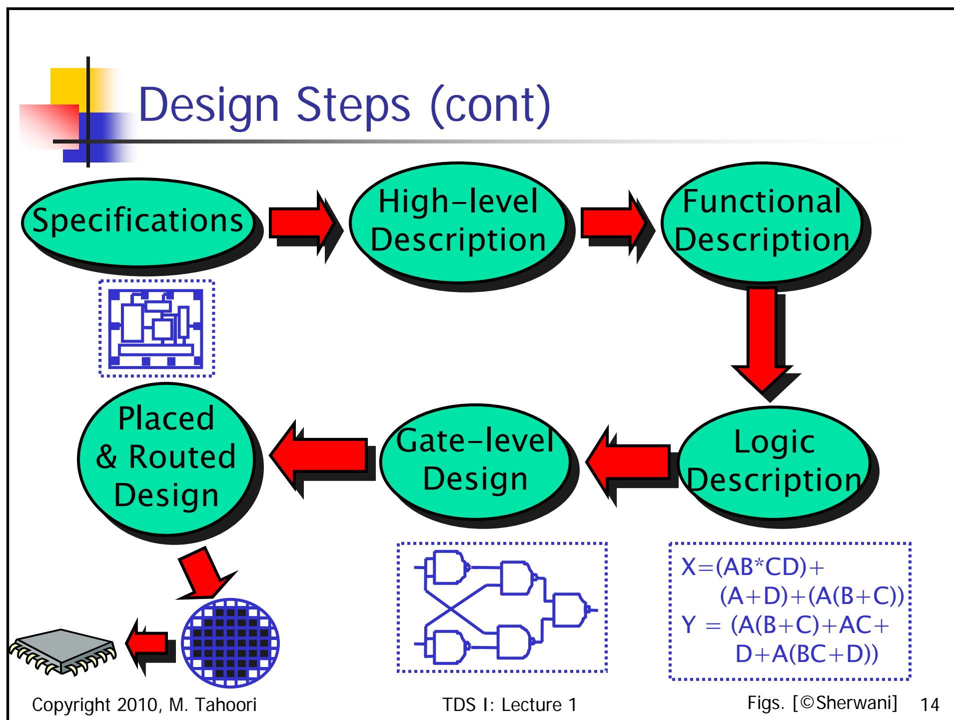


Definitions

- Design synthesis:
  - Given an Input-Output function, develop a procedure to manufacture a device using known materials and processes
- Verification:
  - Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given Input-Output function

Copyright 2010, M. Tahoori TDS I: Lecture 1 12


Design Steps
Specifications
High-level Description
Functional Description
Behavioral VHDL, C
Structural VHDL
Copyright 2010, M. Tahoori
TDS I: Lecture 1
Figs. [©Sherwani]
13


Design Steps (cont)
Specifications
High-level Description
Functional Description
Logic Description
Gate-level Design
Placed & Routed Design
X=(AB*CD)+
(A+D)+(A(B+C))
Y = (A(B+C)+AC+
D+A(BC+D))
Copyright 2010, M. Tahoori
TDS I: Lecture 1
Figs. [©Sherwani]
14

Testing

- The process of determining whether a piece of device
  - Is functioning correctly, or
  - Is defective (broken or faulty)
- Equipment can be defective because it doesn't function
  - as designed, or
  - as specified

Copyright 2010, M. Tahoori

Testing (cont)

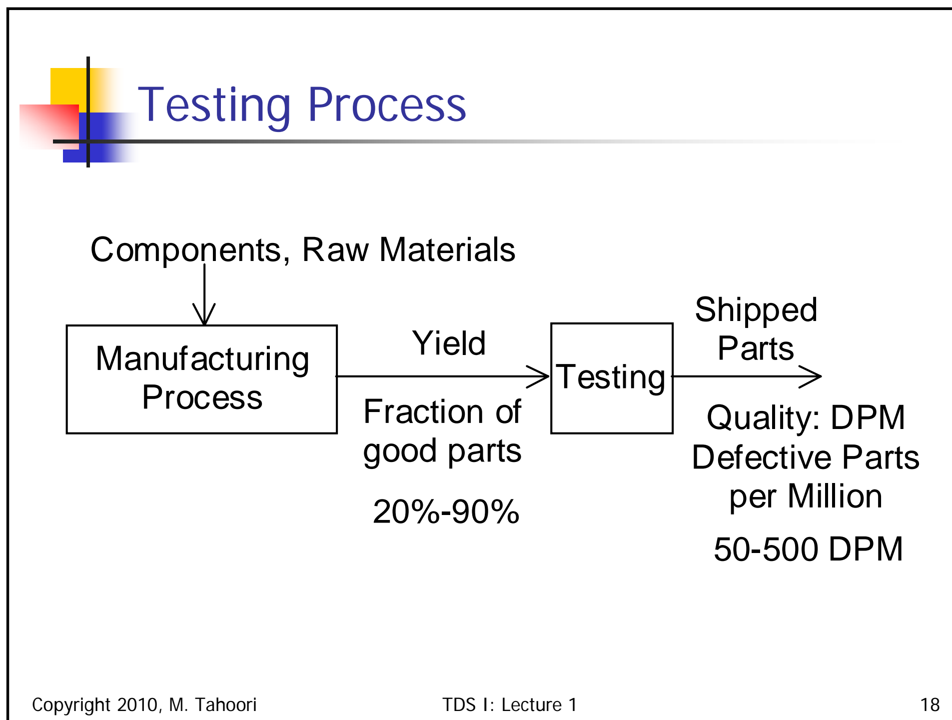
- The need for test depends on
  - Process yield, Y,
    - the proportion of finished units that are not defective
    - Depends on maturity of the manufacturing process, size of the integrated circuit chips and the characteristics of the implemented design, etc.
  - Acceptable quality level (AQL)
    - the planned minimum fraction of defective shipped units
    - Defective Parts per Million (DPM)
    - Depends on the volume of the product, criticality of the applications and the cost of the parts

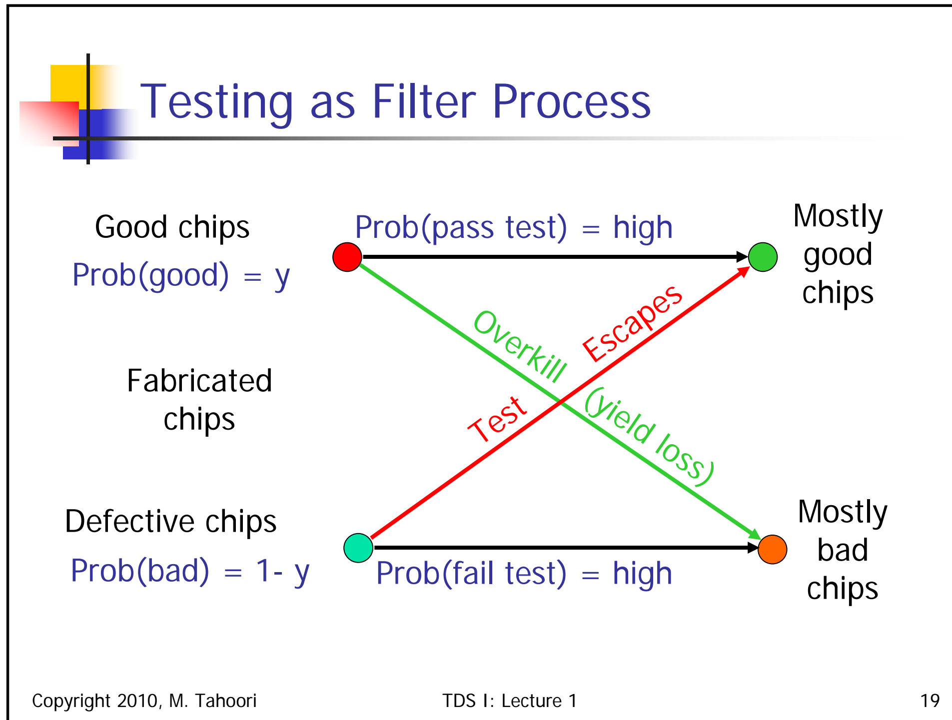
Copyright 2010, M. Tahoori

Yield and Quality Level

- Y and AQL are rarely exactly known
  - Statistically estimated
  - Not feasible to thoroughly test all parts
- Process yield is typically less than AQL
  - defective units must be identified and removed so as to increase the percentage of good units shipped to the customer.

Testing Process

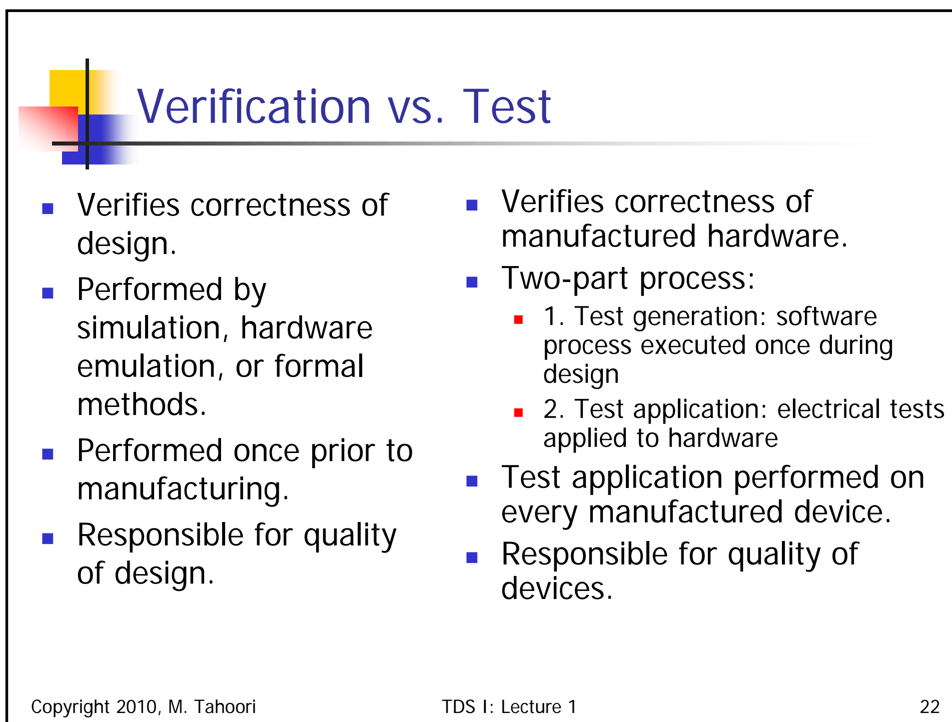


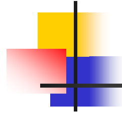


A Part Fails to Operate

- Design Does Not Correspond to Specification
  - Logic Design Incorrect
  - Physical Design Incorrect
- Physical Part Does Not Correspond to Design
  - Manufacturing Defect Present
  - Wear Out Defect Present
- External or Environmental Disturbance
  - Transient Disturbance
  - Power or Temperature Specification Violated

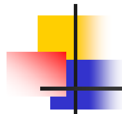
Logic Design Verification
Specification
Behavioral or Register Transfer
Table of Combinations – Boolean Function
Sequential Circuit or State Machine Flow Table
Simulation Vectors and Responses
Informal Word Description of Functionality
Verification Technique
Synthesis
Matching of Two Design Paths
Simulation — Emulation
Formal Verification
Copyright 2010, M. Tahoori
TDS I: Lecture 1
21


Verification vs. Test
Verifies correctness of design.
Performed by simulation, hardware emulation, or formal methods.
Performed once prior to manufacturing.
Responsible for quality of design.
Verifies correctness of manufactured hardware.
Two-part process:
1. Test generation: software process executed once during design
2. Test application: electrical tests applied to hardware
Test application performed on every manufactured device.
Responsible for quality of devices.
Copyright 2010, M. Tahoori
TDS I: Lecture 1
22



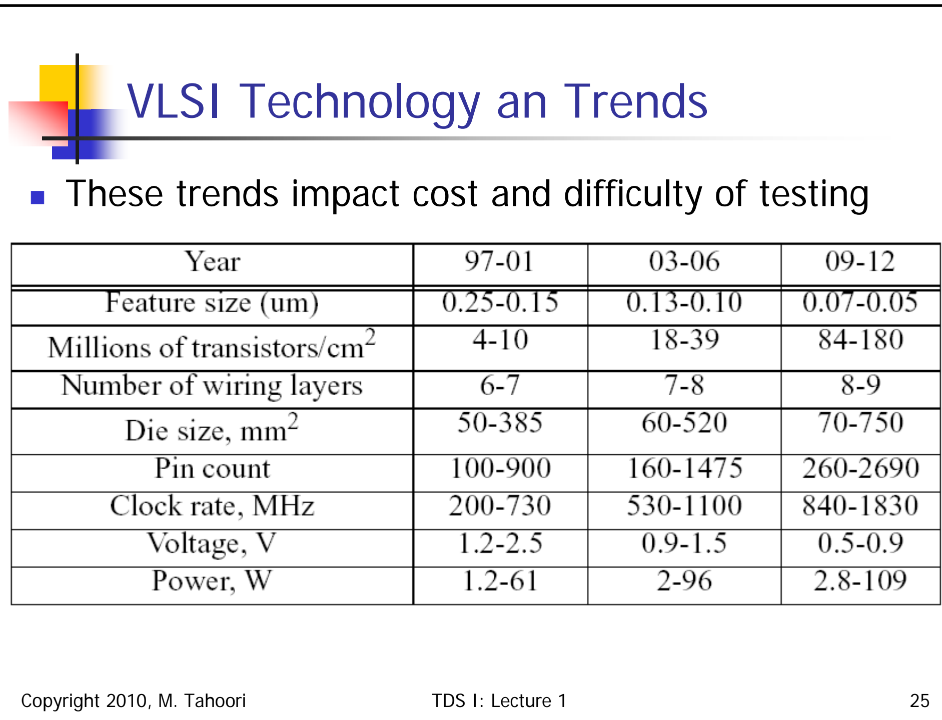
Problems of Ideal Tests

- Definition
  - Ideal tests detect all defects produced in the manufacturing process.
  - Ideal tests pass all functionally good devices.
- Problems
  - Very large numbers and varieties of possible defects need to be tested.
  - Difficult to generate tests for some real defects.
  - Unacceptable test costs
    - Test generation effort, test application time

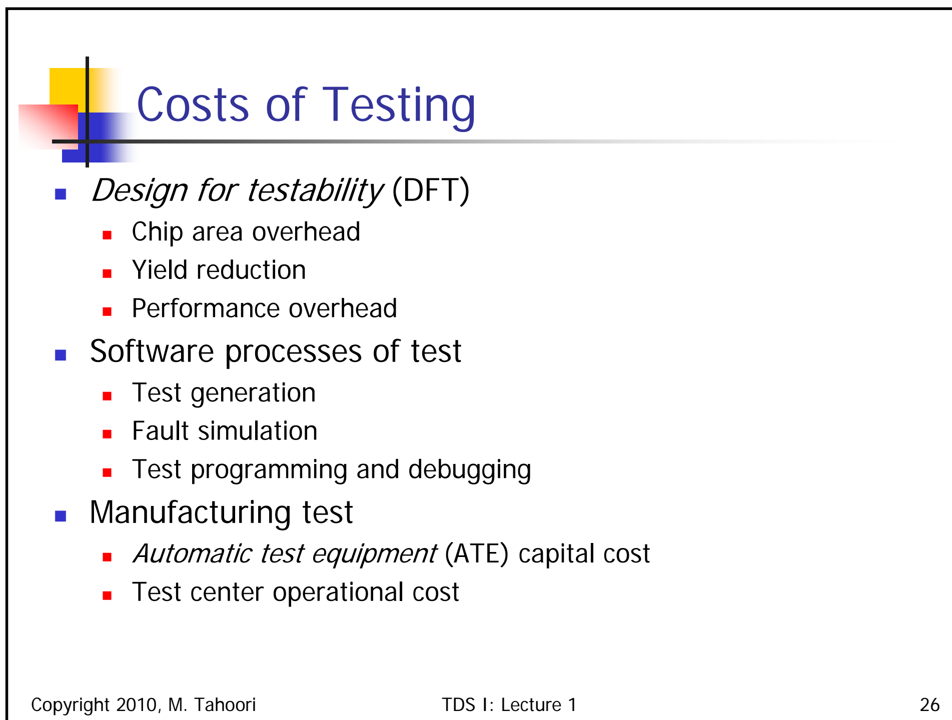


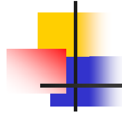
Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected
  - The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests
  - The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*



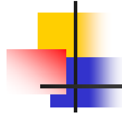
Year	97-01	03-06	09-12
Feature size (um)	0.25-0.15	0.13-0.10	0.07-0.05
Millions of transistors/cm^2	4-10	18-39	84-180
Number of wiring layers	6-7	7-8	8-9
Die size, mm^2	50-385	60-520	70-750
Pin count	100-900	160-1475	260-2690
Clock rate, MHz	200-730	530-1100	840-1830
Voltage, V	1.2-2.5	0.9-1.5	0.5-0.9
Power, W	1.2-61	2-96	2.8-109



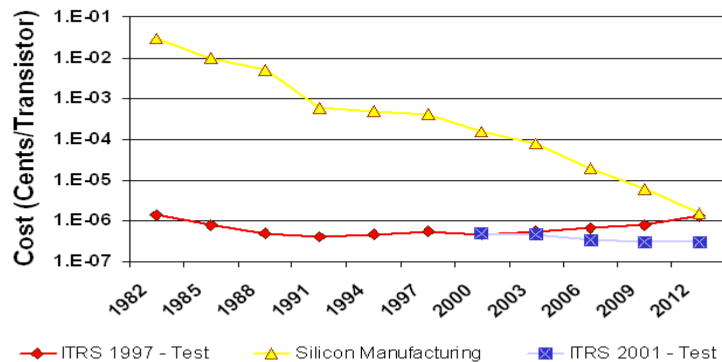


Example: Cost of Testing

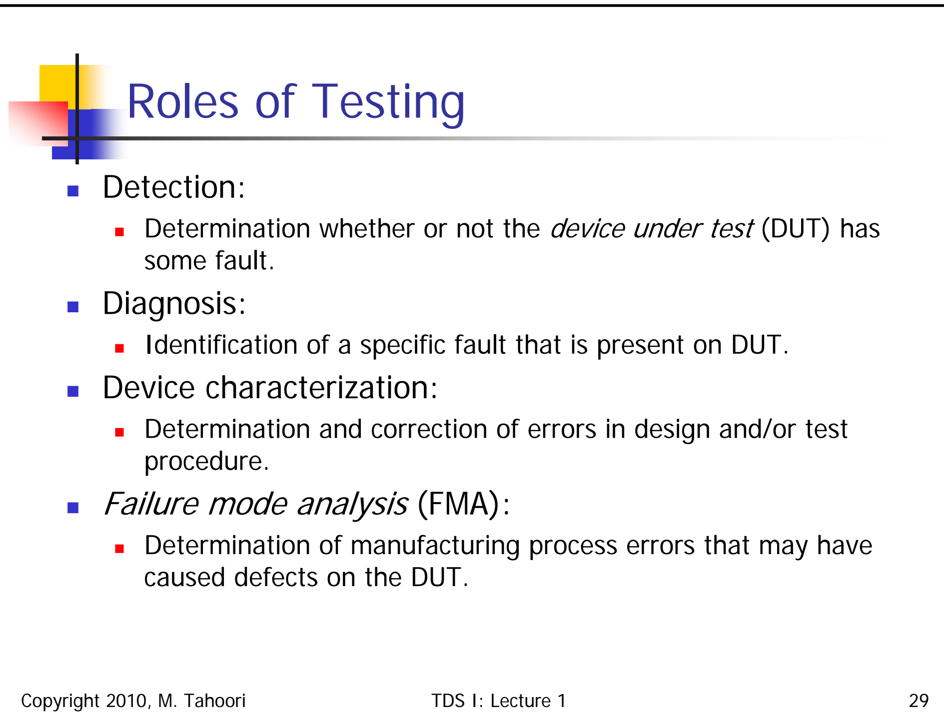
- 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price
  - = \$1.2M + 1,024 x \$3,000 = \$4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = \$0.854M + \$0.085M + \$0.5M
  - = \$1.439M/year
- Test cost (24 hour ATE operation)
  - = \$1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second
- Digital ASIC test time: 6 seconds or 27 cents

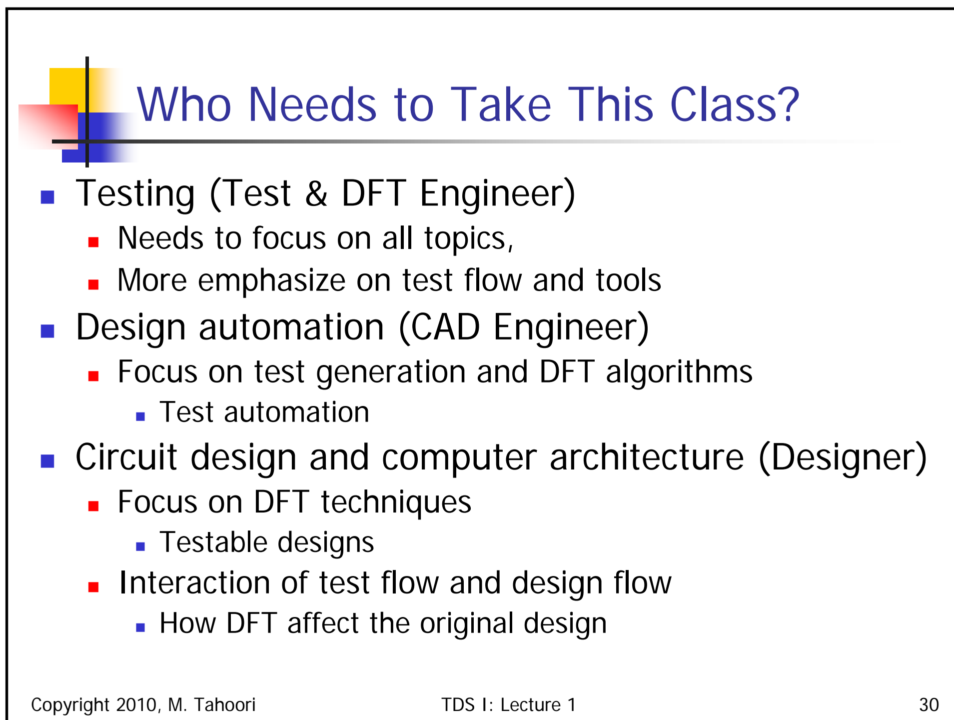


Cost of Manufacturing Test



Source: International Technology Roadmap for Semiconductor Industry (ITRS)


Roles of Testing
Detection:
Determination whether or not the device under test (DUT) has some fault.
Diagnosis:
Identification of a specific fault that is present on DUT.
Device characterization:
Determination and correction of errors in design and/or test procedure.
Failure mode analysis (FMA):
Determination of manufacturing process errors that may have caused defects on the DUT.
Copyright 2010, M. Tahoori
TDS I: Lecture 1
29


Who Needs to Take This Class?
Testing (Test & DFT Engineer)
Needs to focus on all topics,
More emphasize on test flow and tools
Design automation (CAD Engineer)
Focus on test generation and DFT algorithms
Test automation
Circuit design and computer architecture (Designer)
Focus on DFT techniques
Testable designs
Interaction of test flow and design flow
How DFT affect the original design
Copyright 2010, M. Tahoori
TDS I: Lecture 1
30