


Testing Digital Systems I

Lecture 1: Introduction

Instructor: M. Tahoori


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Today's Lecture

- Logistics
- Course Outline
- Introduction


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Logistics

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- Lecture:
 - When: Wednesdays 14:00-15:30
 - Where: Room -118, Building 50.34

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Logistics (cont)

- Requirements
 - Logic Design
 - Computer Architecture
- Background on (preferred but not required)
 - Algorithms and Programming
 - Hardware description languages (VHDL or Verilog)

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Reference Books

- Textbook
 - **Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits** by M. L. Bushnell and V.D. Agrawal, *Kluwer Academic Press*, Boston 2000
- Recommended
 - **System On Chip Test Architectures: Nanometer Design for Testability** by L.T. Wang, C.E. Stroud, N. A. Touba, Elsevier, Morgan Kaufmann Publishers, 2009.
 - **Digital System Testing and Testable Design** by M. Abramovici, M. A. Breuer, and A.D. Friedman, *IEEE Press*, New York, 1990, 652 pages



Course Outline

- Basics
- Test generation methods
- Design for Testability (DFT)

- I try to be flexible. The order and contents may be changed as we proceed.



Outline: Basics

- Introduction
- Failures and errors
- Fault models
- Functional vs Structural testing



Outline: Test Generation

- Test generation techniques and algorithms for combinational logic
- Essentials of test generation methods for sequential circuits
- Logic and fault simulation

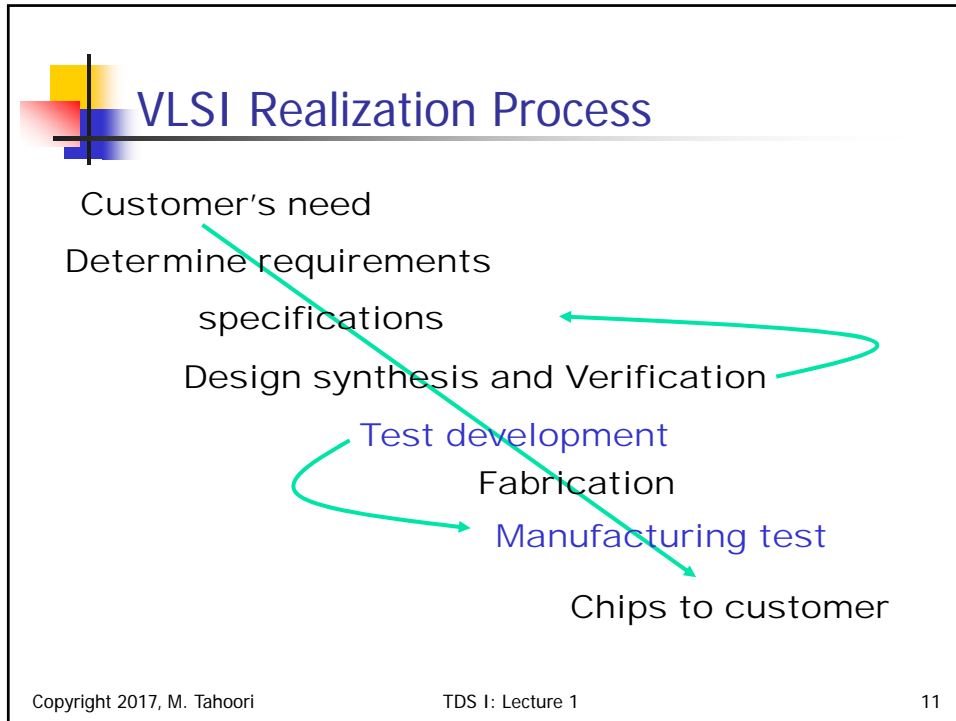


Outline: Design For Testability (DFT)

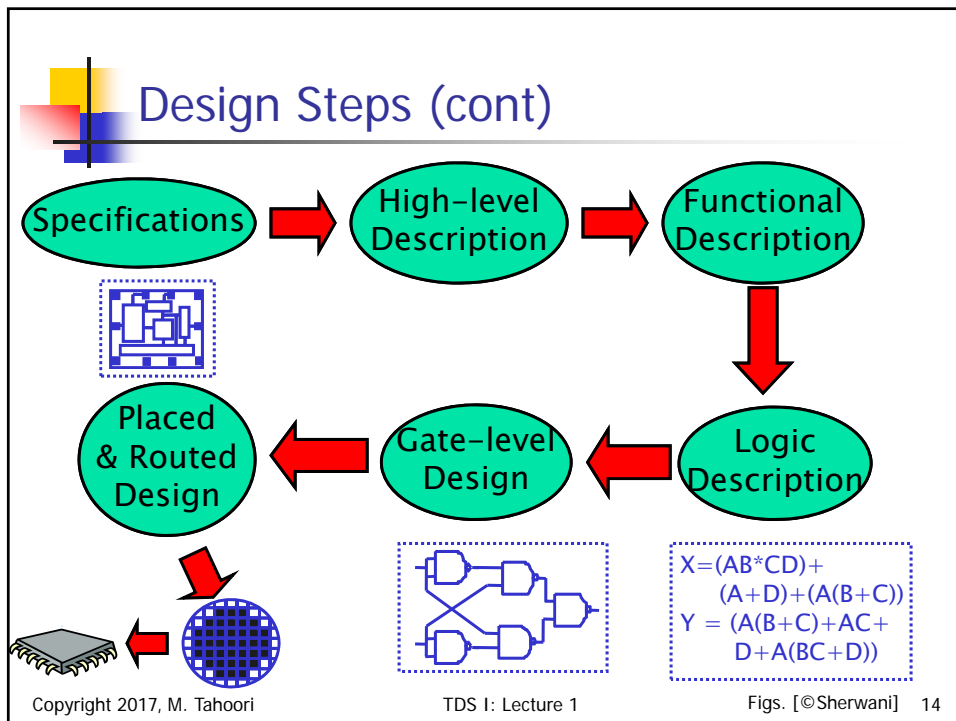
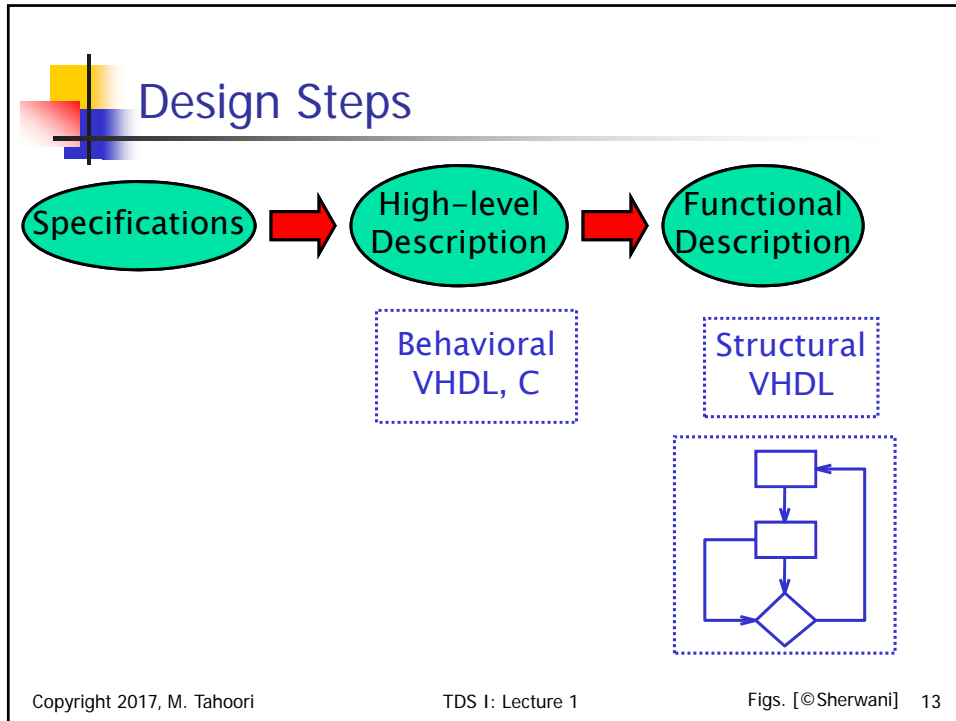
- Ad hoc DFT techniques
- Internal scan design
- Boundary scan



Introduction



-
- Definitions**
- Design synthesis:
 - Given an Input-Output function, develop a procedure to manufacture a device using known materials and processes
 - Verification:
 - Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given Input-Output function
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Testing

- The process of determining whether a piece of device
 - Is functioning correctly, or
 - Is defective (broken or faulty)
- Equipment can be defective because it doesn't function
 - as designed, or
 - as specified



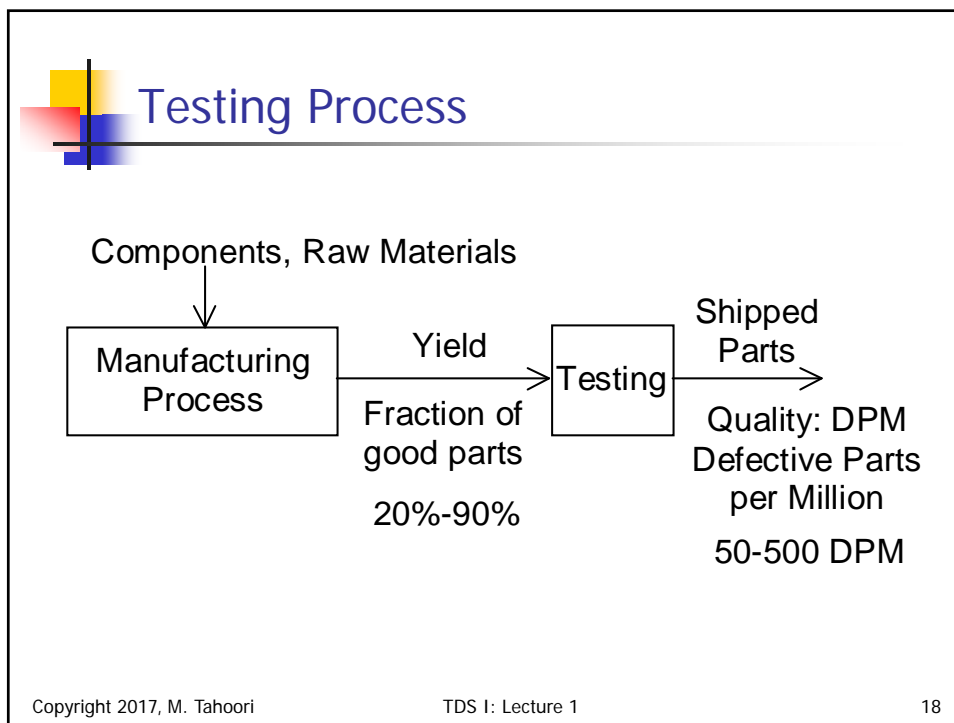
Testing (cont)

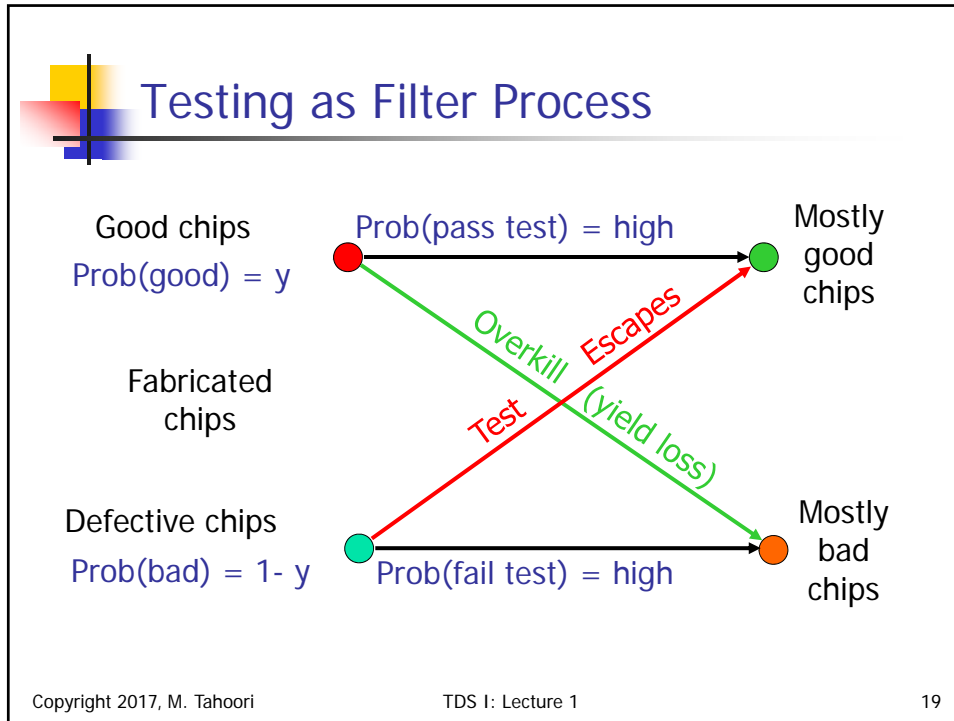
- The need for test depends on
 - Process yield, Y ,
 - the proportion of finished units that are not defective
 - Depends on maturity of the manufacturing process, size of the integrated circuit chips and the characteristics of the implemented design, etc.
 - Acceptable quality level (AQL)
 - the planned minimum fraction of defective shipped units
 - Defective Parts per Million (DPM)
 - Depends on the volume of the product, criticality of the applications and the cost of the parts

Yield and Quality Level

- Y and AQL are rarely exactly known
 - Statistically estimated
 - Not feasible to thoroughly test all parts
- Process yield is typically less than AQL
 - defective units must be identified and removed so as to increase the percentage of good units shipped to the customer.

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- ### A Part Fails to Operate
- Design Does Not Correspond to Specification
 - Logic Design Incorrect
 - Physical Design Incorrect
 - Physical Part Does Not Correspond to Design
 - Manufacturing Defect Present
 - Wear Out Defect Present
 - External or Environmental Disturbance
 - Transient Disturbance
 - Power or Temperature Specification Violated
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Logic Design Verification

- Specification
 - Behavioral or Register Transfer
 - Table of Combinations – Boolean Function
 - Sequential Circuit or State Machine Flow Table
 - Simulation Vectors and Responses
 - Informal Word Description of Functionality
- Verification Technique
 - Synthesis
 - Matching of Two Design Paths
 - Simulation — Emulation
 - Formal Verification

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Verification vs. Test

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.
- Verifies correctness of manufactured hardware.
- Two-part process:
 - 1. Test generation: software process executed once during design
 - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

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Problems of Ideal Tests

- Definition
 - Ideal tests detect all defects produced in the manufacturing process.
 - Ideal tests pass all functionally good devices.
- Problems
 - Very large numbers and varieties of possible defects need to be tested.
 - Difficult to generate tests for some real defects.
 - Unacceptable test costs
 - Test generation effort, test application time



Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected
 - The fraction (or percentage) of such chips is called the *yield loss*.
- Some bad chips pass tests
 - The fraction (or percentage) of bad chips among all passing chips is called the *defect level*.



VLSI Technology an Trends

- These trends impact cost and difficulty of testing

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Logic trans/cm ²	6.2M	18M	39M	84M	180M	390M
Cost/trans (mc)	1.735	.580	.255	.110	.049	.022
#pads/chip	1867	2553	3492	4776	6532	8935
Clock (MHz)	1250	2100	3500	6000	10000	16900
Chip size (mm ²)	340	430	520	620	750	900
Wiring levels	6-7	7	7-8	8-9	9	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.5
High-perf pow (W)	90	130	160	170	175	183



Costs of Testing

- *Design for testability* (DFT)
 - Chip area overhead
 - Yield reduction
 - Performance overhead
- Software processes of test
 - Test generation
 - Fault simulation
 - Test programming and debugging
- Manufacturing test
 - *Automatic test equipment* (ATE) capital cost
 - Test center operational cost

Example: Cost of Testing

- 0.5-1.0GHz, analog instruments, 1,024 digital pins:
ATE purchase price
 - = $\$1.2\text{M} + 1,024 \times \$3,000 = \$4.272\text{M}$
- Running cost (five-year linear depreciation)
 - = Depreciation + Maintenance + Operation
 - = $\$0.854\text{M} + \$0.085\text{M} + \$0.5\text{M}$
 - = $\$1.439\text{M}/\text{year}$
- Test cost (24 hour ATE operation)
 - = $\$1.439\text{M}/(365 \times 24 \times 3,600)$
 - = 4.5 cents/second
- Digital ASIC test time: 6 seconds or 27 cents


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Cost of Manufacturing Test

Year	ITRS 1997 - Test (Cents/Transistor)	Silicon Manufacturing (Cents/Transistor)	ITRS 2001 - Test (Cents/Transistor)
1982	~1.E-06	~1.E-02	-
1985	~1.E-06	~1.E-03	-
1988	~1.E-06	~1.E-03	-
1991	~1.E-06	~1.E-03	-
1994	~1.E-06	~1.E-03	-
1997	~1.E-06	~1.E-03	-
2000	~1.E-06	~1.E-04	~1.E-06
2003	~1.E-06	~1.E-04	~1.E-06
2006	~1.E-06	~1.E-05	~1.E-06
2009	~1.E-06	~1.E-05	~1.E-06
2012	~1.E-06	~1.E-06	~1.E-06

Source: International Technology Roadmap for Semiconductor Industry (ITRS)


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Roles of Testing

- **Detection:**
 - Determination whether or not the *device under test* (DUT) has some fault.
- **Diagnosis:**
 - Identification of a specific fault that is present on DUT.
- **Device characterization:**
 - Determination and correction of errors in design and/or test procedure.
- **Failure mode analysis (FMA):**
 - Determination of manufacturing process errors that may have caused defects on the DUT.

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Who Needs to Take This Class?

- **Testing (Test & DFT Engineer)**
 - Needs to focus on all topics,
 - More emphasize on test flow and tools
- **Design automation (CAD Engineer)**
 - Focus on test generation and DFT algorithms
 - Test automation
- **Circuit design and computer architecture (Designer)**
 - Focus on DFT techniques
 - Testable designs
 - Interaction of test flow and design flow
 - How DFT affect the original design

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CDNC Teaching Modules

Labs

- FPGA Programming
 - Introduction to FPGAs
 - Circuit development for FPGAs
 - Hands-on experiments with FPGAs

- Intel Galileo Design Lab
 - Introduction to Intel Galileo
 - Circuit development
 - Hands-on experiments



Labs

- Digital Design and Test Flow
 - Introduction to algorithms and tools for Electronic Design Automation
 - The entire design flow from specification to chips

```

    graph TD
      S([Specifications]) --> HD([High-level Description])
      HD --> FD([Functional Description])
      FD --> LD([Logic Description])
      LD --> GLD([Gate-level Design])
      GLD --> PRD([Placed & Routed Design])
      PRD --> Chip[Chip]
      
```

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Seminars

- Non-Volatile Memory Technologies
 - Introduction to non-volatile memories
 - Can these be used to replace SRAM/DRAM?

- Near Threshold Computing
 - Ultra-low power computing for Internet of Things (IoT) platforms
 - Advantage: Huge power savings
 - Challenge: Performance degradation, reliability issues

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HiWi and Master Projects

- Hiwi positions
 - To help with various research projects in dependable computing
 - Required knowledge
 - Programming
 - Digital design and computer architecture (DT+RO)
- Master Projects
 - Various projects related to
 - Novel computer architecture and logic design
 - Dependable computing
 - Emerging non-volatile memories

Contact us if interested & for more details: cdnc@ira.uka.de