Testing Digital Systems II

Lecture 10:
Logic Diagnosis

Instructor: M. Tahoori

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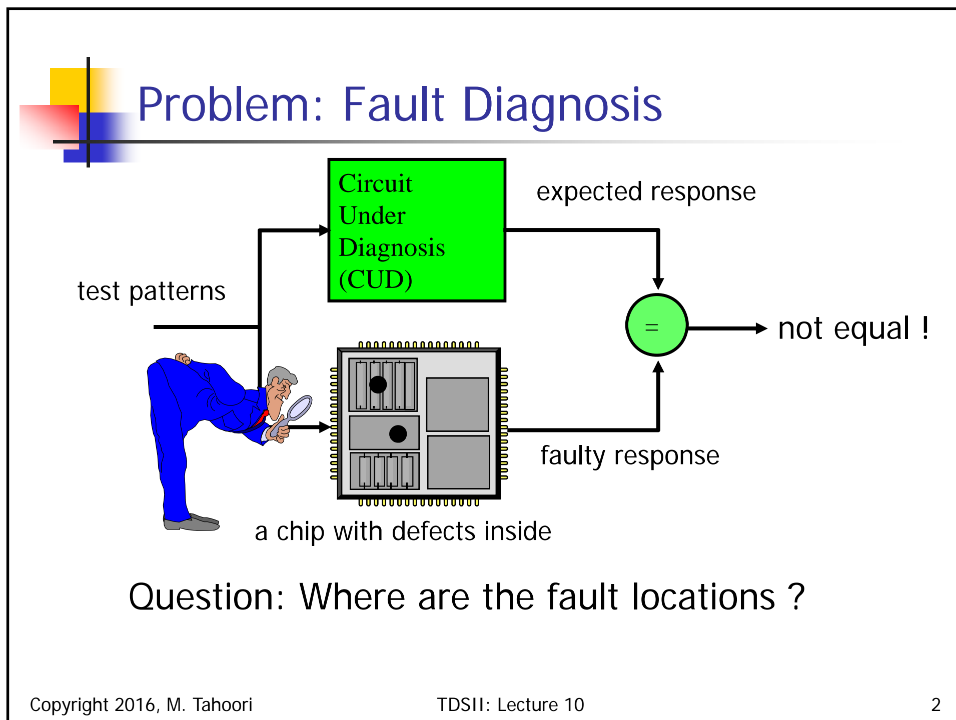
Problem: Fault Diagnosis



Question: Where are the fault locations ?

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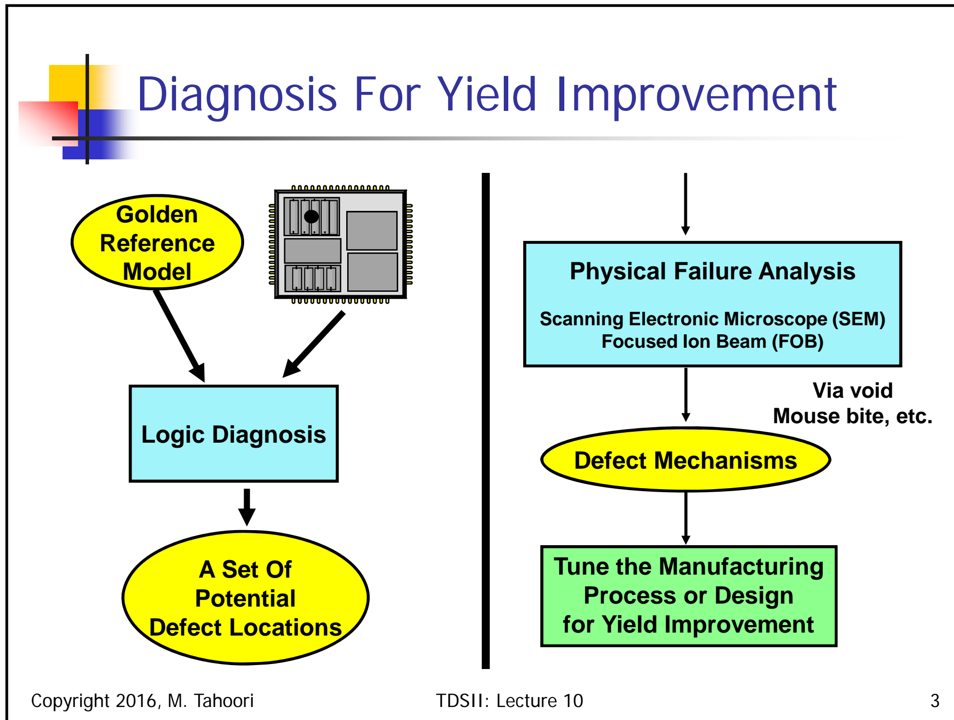
Diagnosis For Yield Improvement
Golden Reference Model
Logic Diagnosis
A Set Of Potential Defect Locations
Physical Failure Analysis
Scanning Electronic Microscope (SEM)
Focused Ion Beam (FOB)
Via void
Mouse bite, etc.
Defect Mechanisms
Tune the Manufacturing Process or Design for Yield Improvement
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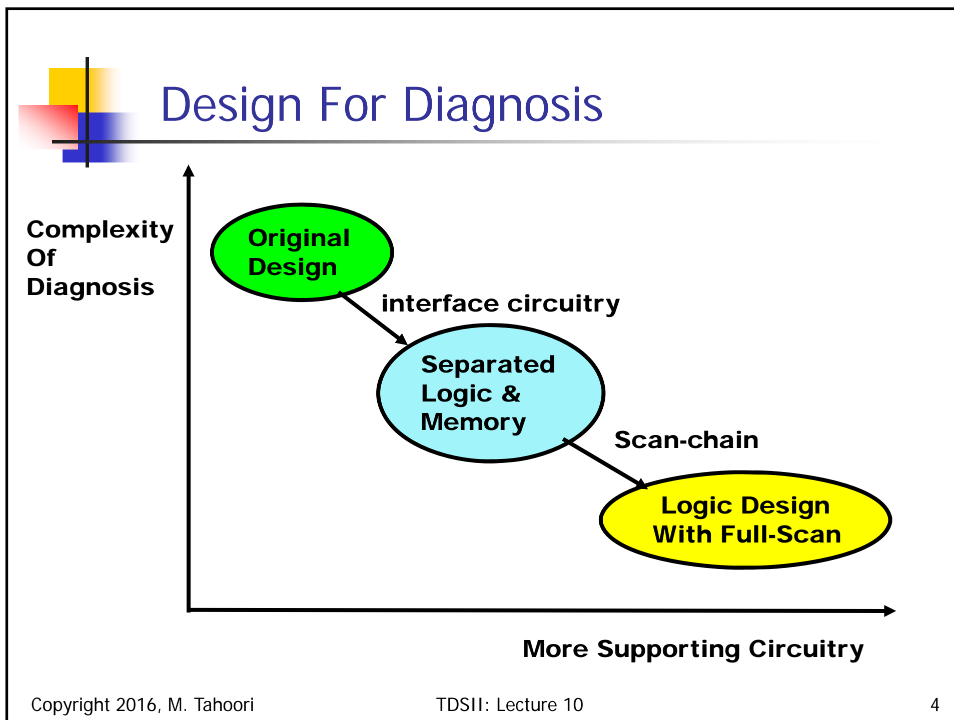
Design For Diagnosis
Complexity Of Diagnosis
Original Design
interface circuitry
Separated Logic & Memory
Scan-chain
Logic Design With Full-Scan
More Supporting Circuitry
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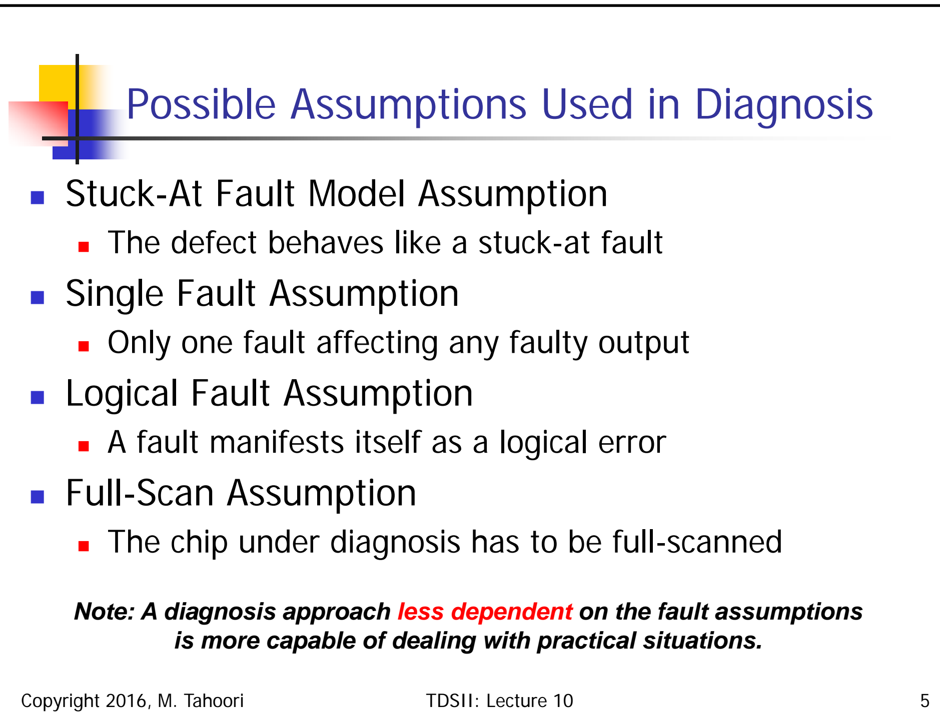
Possible Assumptions Used in Diagnosis
Stuck-At Fault Model Assumption
The defect behaves like a stuck-at fault
Single Fault Assumption
Only one fault affecting any faulty output
Logical Fault Assumption
A fault manifests itself as a logical error
Full-Scan Assumption
The chip under diagnosis has to be full-scanned
Note: A diagnosis approach less dependent on the fault assumptions is more capable of dealing with practical situations.
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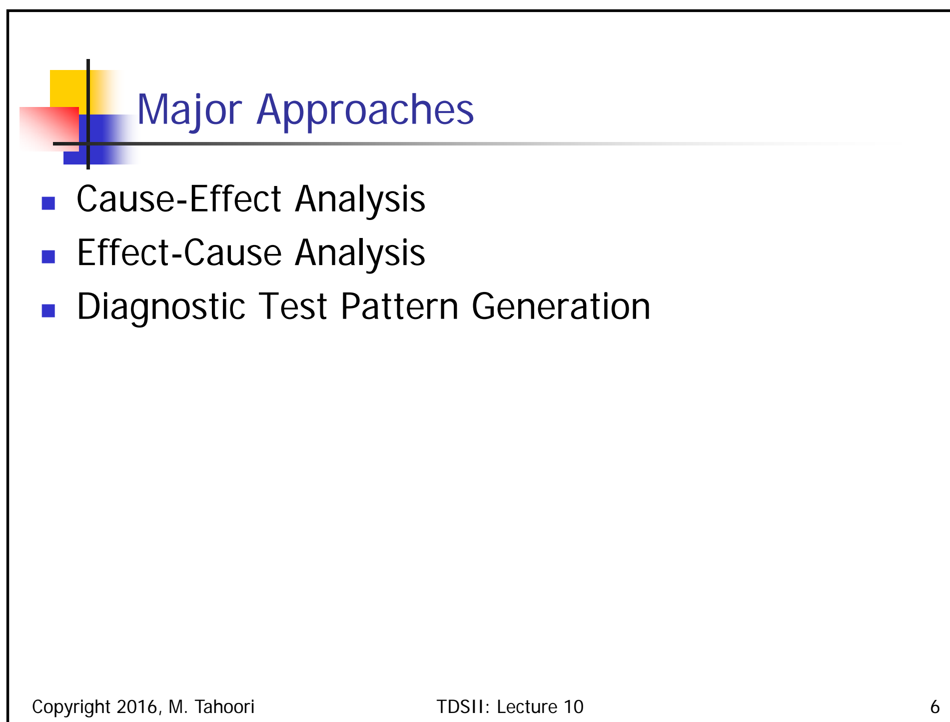
Major Approaches
Cause-Effect Analysis
Effect-Cause Analysis
Diagnostic Test Pattern Generation
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Terminology

- **Device Under Diagnosis (DUD): The Failing Chip**
- **Circuit Under Diagnosis (CUD): The Circuit Model**
- **Failing Input Vector: Causes Mismatches**

Failing chip

input vector v

X mismatched PO
O matched PO
O matched PO
O matched PO
X mismatched PO

Gate-level CUD

Cause-Effect Analysis

- Fault dictionary (pre-analysis of all causes)
  - Records test response of every fault under the applied test set
  - Built by intensive fault simulation process
- A chip is diagnosed (effect matching)
  - By matching up the failing syndromes observed at the tester with the pre-stored fault dictionary

Fault Dictionary Example

A diagnosis session: traverse from a path from root to a leaf

a, b, c → Circuit under Diagnosis → g

(a) Circuit under diagnosis

Circuits	Test vectors in terms of (a, b, c)				
	v_1	v_2	v_3	v_4	v_5
fault-free	0	0	0	0	1
f_1	0	1	1	1	1
f_2	1	1	1	0	1
f_3	1	0	0	1	1
f_4	0	0	1	0	0
f_5	0	1	1	0	1

(b) Full-response dictionary

$\{f_1, f_2, f_3, f_4, f_5\}$ — v_1: output=0 → $\{f_1, f_4, f_5\}$; output=1 → $\{f_2, f_3\}$

$\{f_1, f_4, f_5\}$ — v_2: 0 → f_4; 1 → $\{f_1, f_5\}$

$\{f_2, f_3\}$ — v_2: 0 → f_3; 1 → f_2

$\{f_1, f_5\}$ — v_4: 0 → f_5; 1 → f_1

(c) Diagnostic tree

Terminology: Mismatched Output

Effect-cause analysis does not build fault dictionary
It predicts fault locations by analyzing CUD from mismatch PO's

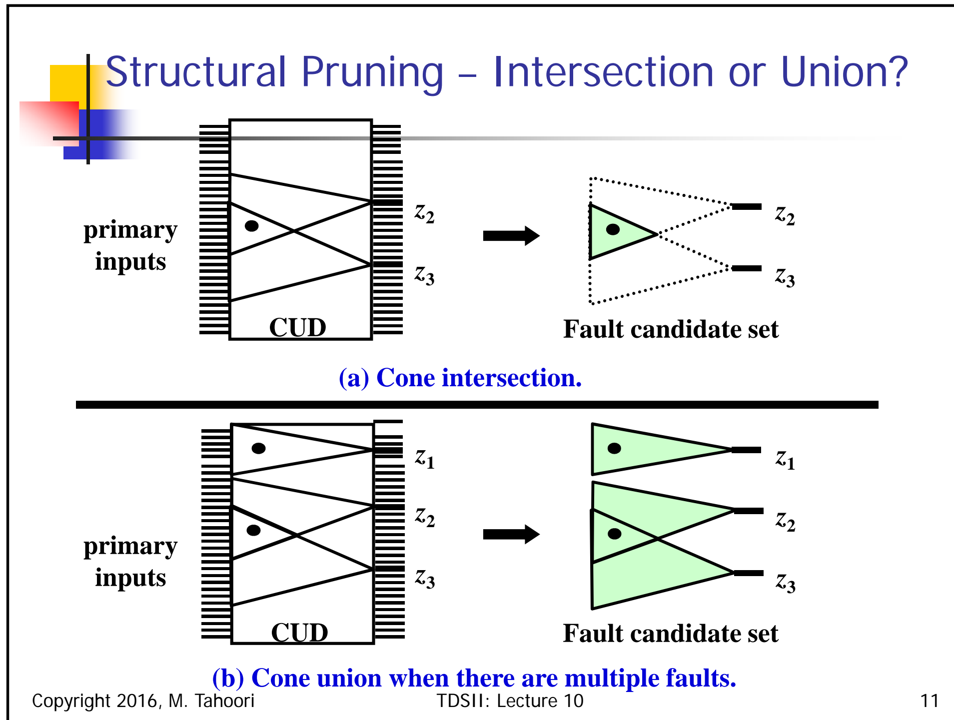
failing chip

0 failing PO
0
0
0
0 failing PO

input vector v

CUD

1 mismatched PO
0
0
0
1 mismatched PO


Structural Pruning – Intersection or Union?
primary inputs
CUD
z_2
z_3
Fault candidate set
(a) Cone intersection.
primary inputs
CUD
z_1
z_2
z_3
Fault candidate set
(b) Cone union when there are multiple faults.
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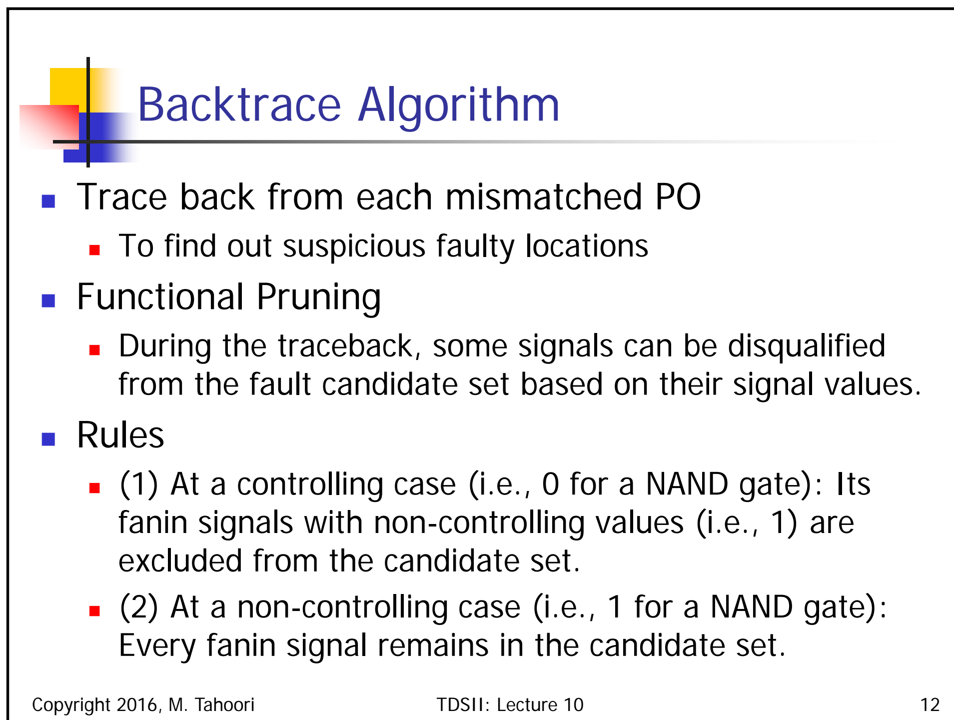
Backtrace Algorithm
Trace back from each mismatched PO
To find out suspicious faulty locations
Functional Pruning
During the traceback, some signals can be disqualified from the fault candidate set based on their signal values.
Rules
(1) At a controlling case (i.e., 0 for a NAND gate): Its fanin signals with non-controlling values (i.e., 1) are excluded from the candidate set.
(2) At a non-controlling case (i.e., 1 for a NAND gate): Every fanin signal remains in the candidate set.
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Backtrace Example

All suspicious fault locations are marked in red.

Target mismatched output

0 1 0 1 1 0 1 1 1 1 0 1
a b c d e f

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Diagnostic Test Pattern Generation

DTPG helps to increase diagnostic resolution

fault-free circuit

Model for differentiating vector generation

d_1 stuck-at 1

d_2 stuck-at 0

z/0

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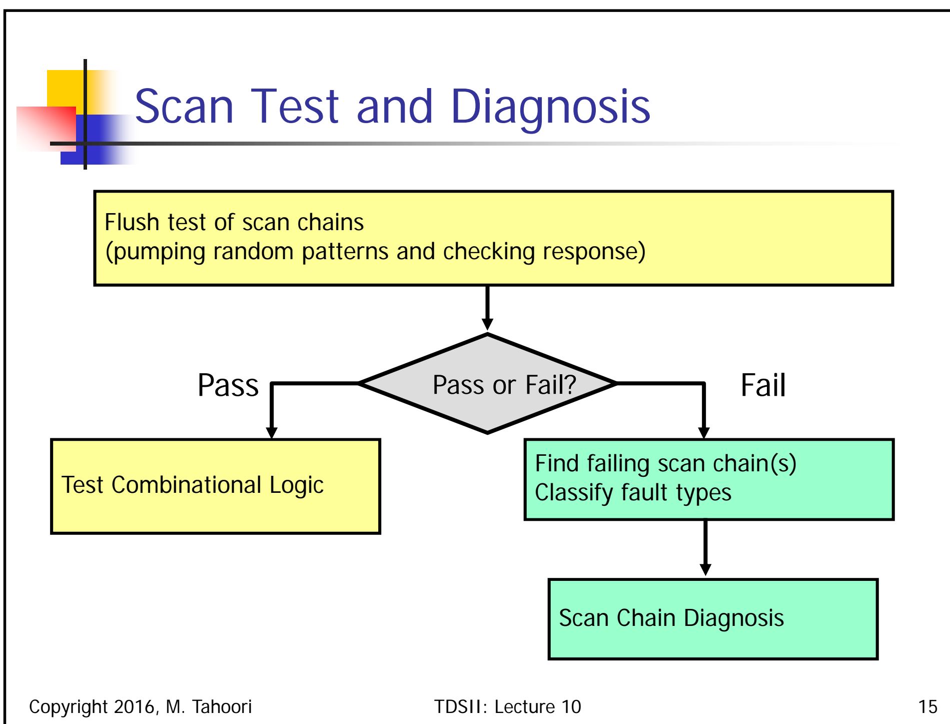
Scan Test and Diagnosis
Flush test of scan chains
(pumping random patterns and checking response)
Pass or Fail?
Pass
Fail
Test Combinational Logic
Find failing scan chain(s)
Classify fault types
Scan Chain Diagnosis
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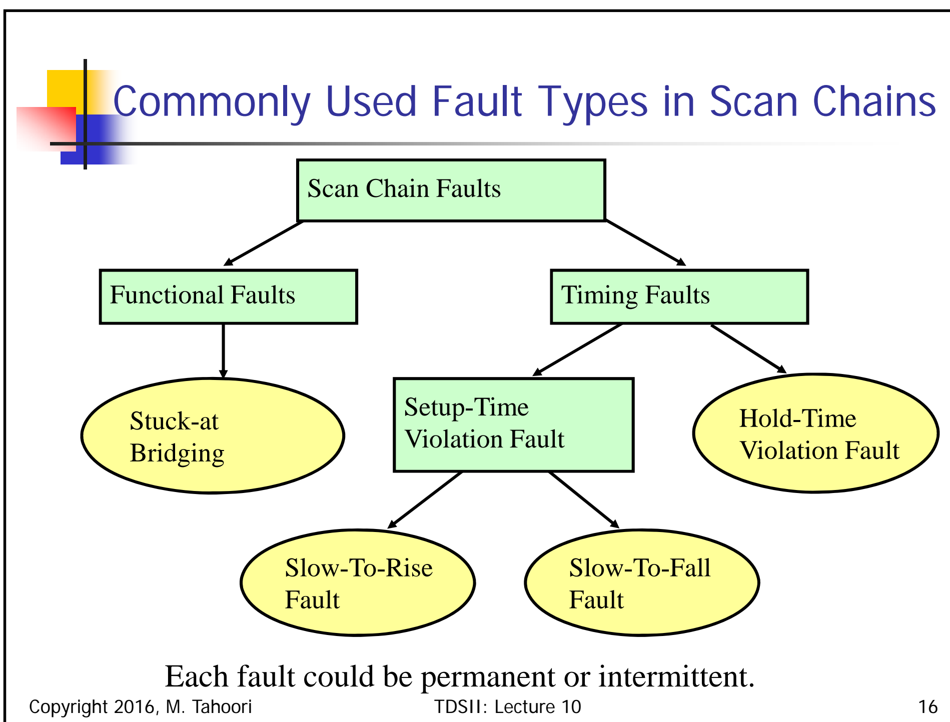
Commonly Used Fault Types in Scan Chains
Scan Chain Faults
Functional Faults
Timing Faults
Stuck-at
Bridging
Setup-Time
Violation Fault
Hold-Time
Violation Fault
Slow-To-Rise
Fault
Slow-To-Fall
Fault
Each fault could be permanent or intermittent.
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A Stuck-At Fault In the Chain

Effect: A killer of the scan-test sequence

Combinational Logic

input pins

output pins

scan-input (SI)

11010100

scan-output (SO)

00000000

All-0 syndrome

MUX D Q

s-a-0

?

scan-enable

clock

Example: Faulty Syndrome of a Scan Chain

A scan chain

SI (scan input pin)

SO (scan output pin)

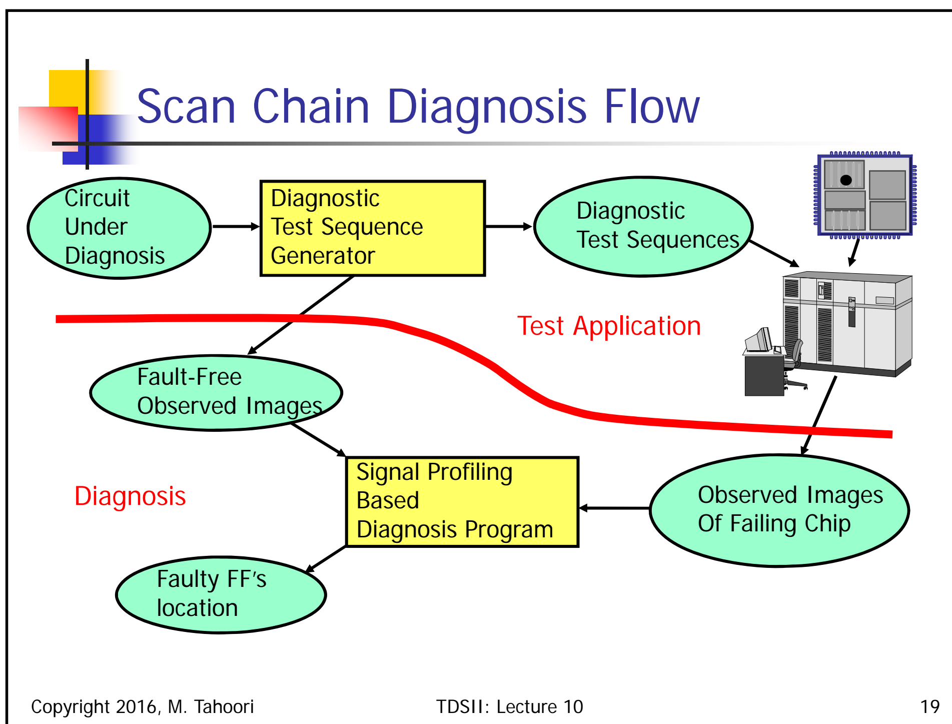
A faulty flip-flop

Fault Type	Scan-In Pattern	Observed Syndrome
Stuck-at-0	1100110011001100	0000000000000000
Stuck-at-1	1100110011001100	1111111111111111
Slow-to-Rise	1100110011001100	1000100010001000
Slow-to-Fall	1100110011001100	1101110111011100

The rightmost bit goes into the scan first

The rightmost bit gets out of the scan first

An underlined bit in the observed image is failing.


Scan Chain Diagnosis Flow
Circuit Under Diagnosis
Diagnostic Test Sequence Generator
Diagnostic Test Sequences
Test Application
Fault-Free Observed Images
Diagnosis
Signal Profiling Based Diagnosis Program
Observed Images Of Failing Chip
Faulty FF's location
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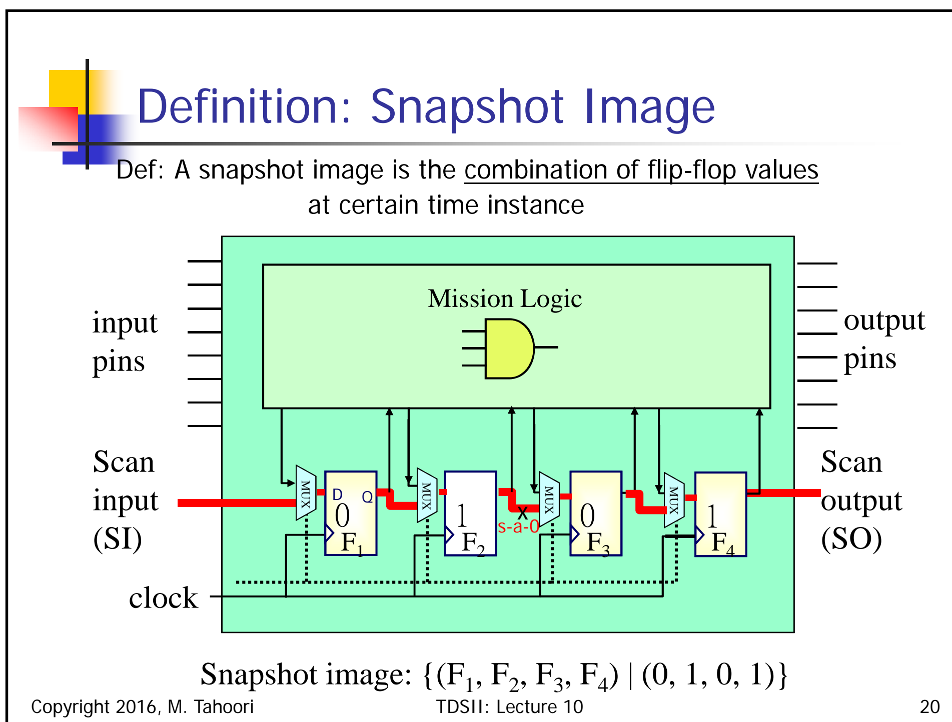
Definition: Snapshot Image
Def: A snapshot image is the combination of flip-flop values at certain time instance
Mission Logic
input pins
output pins
Scan input (SI)
Scan output (SO)
clock
MUX
D
Q
0
1
F1
F2
F3
F4
s-a-0
Snapshot image: {(F1, F2, F3, F4) | (0, 1, 0, 1)}
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Definition: Observed Image

Def: An observed image is the scanned-out version of a snapshot image.

Snapshot image: $\{(F_1, F_2, F_3, F_4) \mid (0, 1, 0, 1)\}$

Observed image: $\{(F_1, F_2, F_3, F_4) \mid (0, 0, 0, 1)\}$

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Modified Inject-and-Evaluate Paradigm

A stuck-at-0 fault is assumed at the output of the 2nd FF from SI

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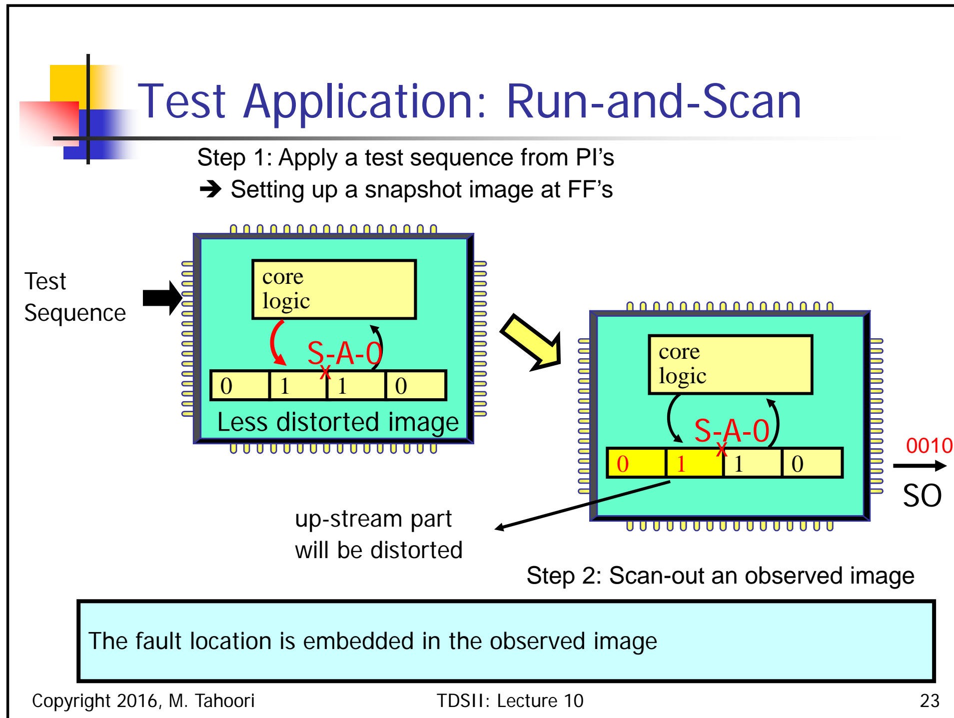
Test Application: Run-and-Scan
Step 1: Apply a test sequence from PI's
➔ Setting up a snapshot image at FF's
Test Sequence
core logic
S-A-0
0 1 1 0
Less distorted image
core logic
S-A-0
0 1 1 0
0010
SO
up-stream part will be distorted
Step 2: Scan-out an observed image
The fault location is embedded in the observed image
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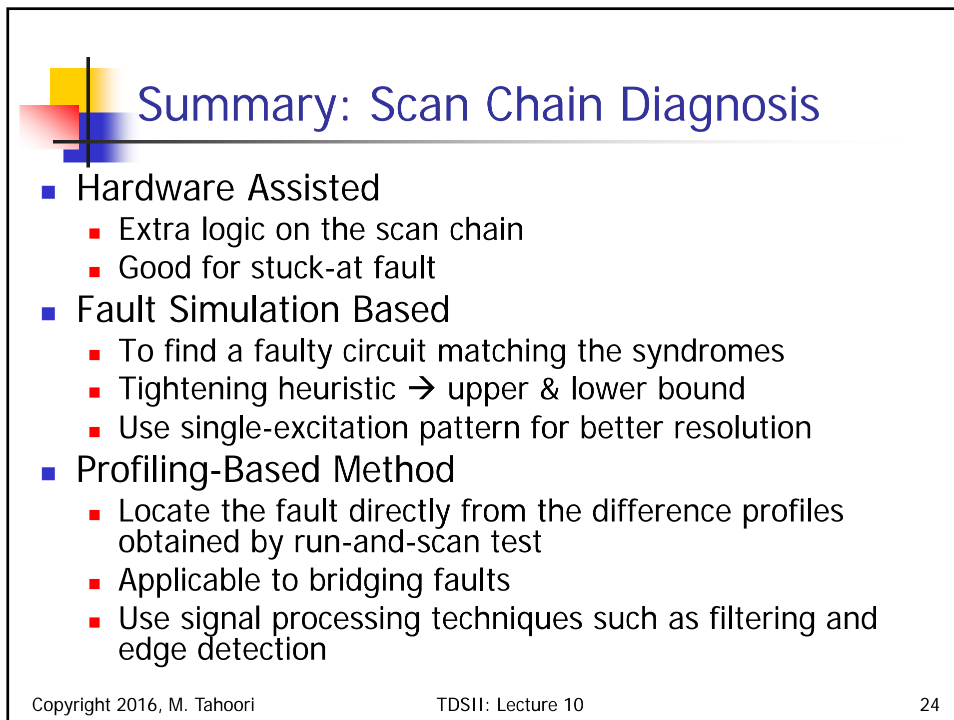
Summary: Scan Chain Diagnosis
Hardware Assisted
Extra logic on the scan chain
Good for stuck-at fault
Fault Simulation Based
To find a faulty circuit matching the syndromes
Tightening heuristic → upper & lower bound
Use single-excitation pattern for better resolution
Profiling-Based Method
Locate the fault directly from the difference profiles obtained by run-and-scan test
Applicable to bridging faults
Use signal processing techniques such as filtering and edge detection
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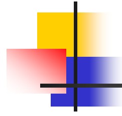
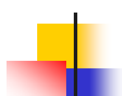
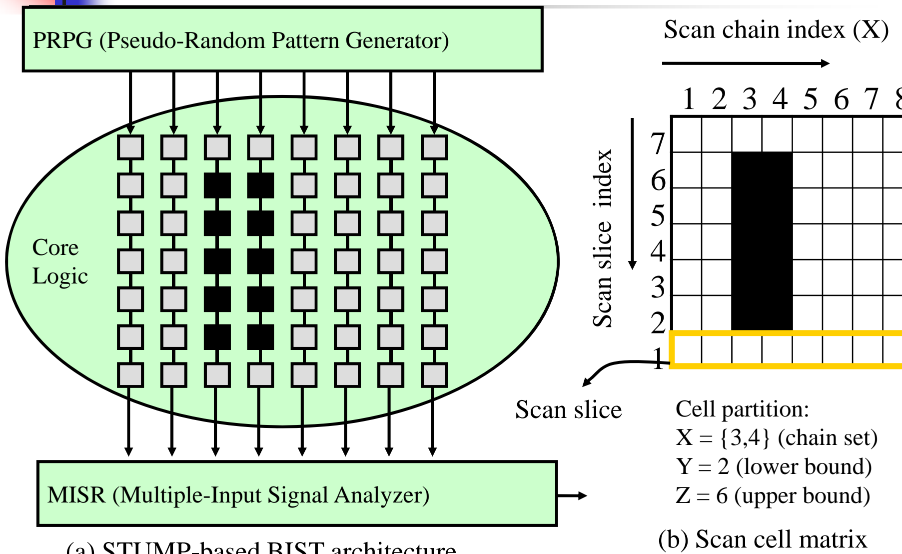


Diagnosis for BIST Logic

- Diagnosis in a BIST environment requires
  - determining from compacted output responses which test vectors have produced a faulty response (**time information**)
  - determining from compacted output responses which scan cells have captured errors (**space information**)
- The true fault location inside the logic
  - Can then be inferred from the above space and time information using combinational logic diagnosis

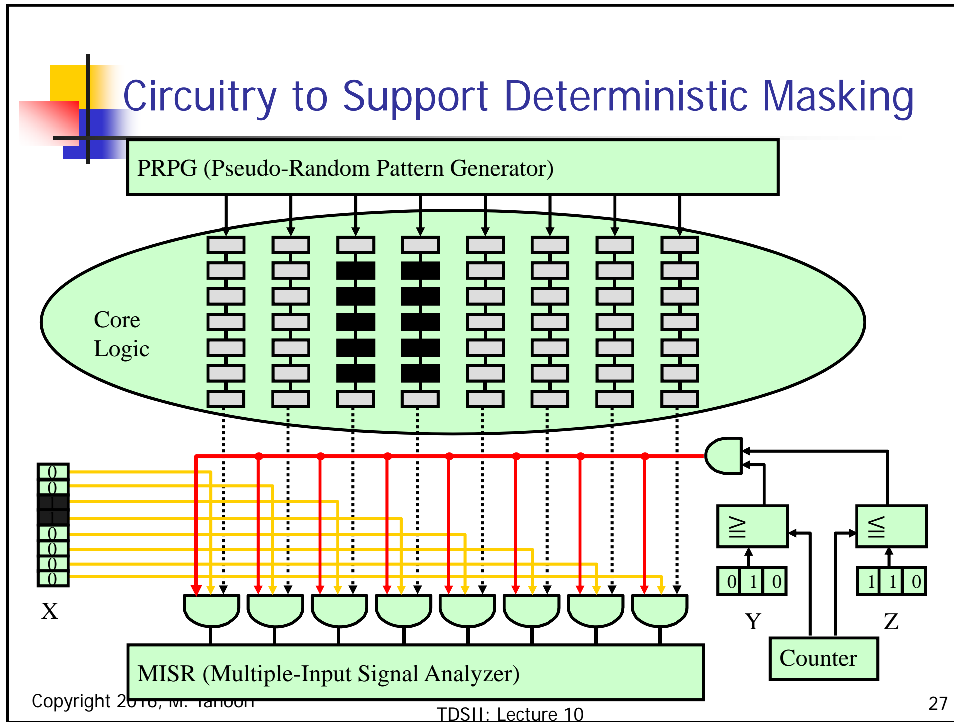


Deterministic Masking-Based Diagnosis



(a) STUMP-based BIST architecture

(b) Scan cell matrix


Circuitry to Support Deterministic Masking
PRPG (Pseudo-Random Pattern Generator)
Core
Logic
X
≥
≤
0 1 0
1 1 0
Y
Z
Counter
MISR (Multiple-Input Signal Analyzer)
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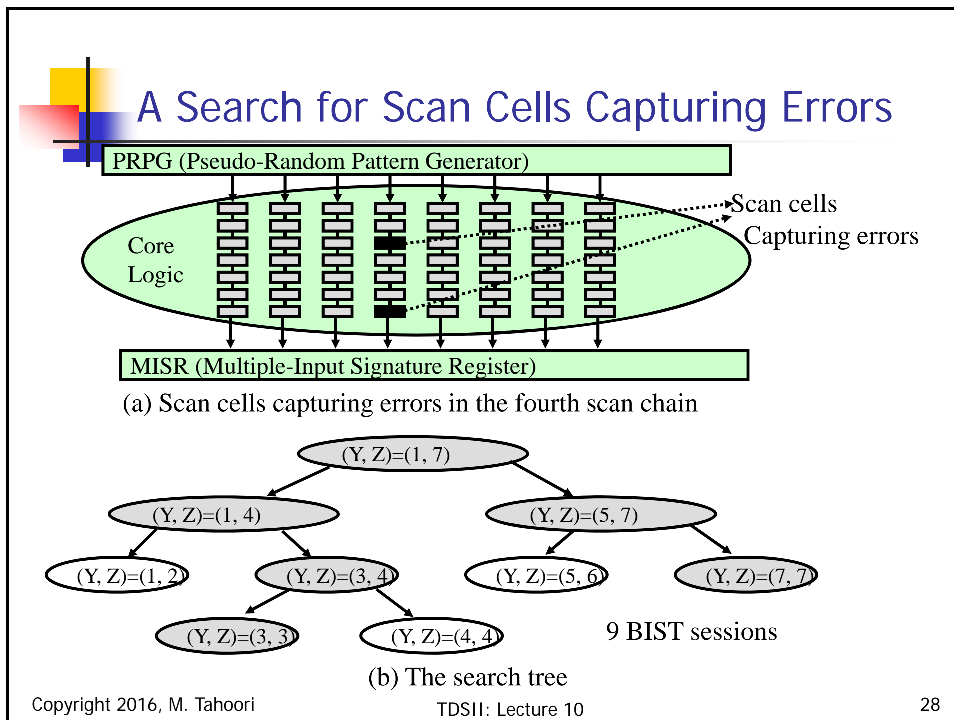
27


A Search for Scan Cells Capturing Errors
PRPG (Pseudo-Random Pattern Generator)
Core
Logic
Scan cells
Capturing errors
MISR (Multiple-Input Signature Register)
(a) Scan cells capturing errors in the fourth scan chain
(Y, Z)=(1, 7)
(Y, Z)=(1, 4)
(Y, Z)=(5, 7)
(Y, Z)=(1, 2)
(Y, Z)=(3, 4)
(Y, Z)=(5, 6)
(Y, Z)=(7, 7)
(Y, Z)=(3, 3)
(Y, Z)=(4, 4)
9 BIST sessions
(b) The search tree
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28