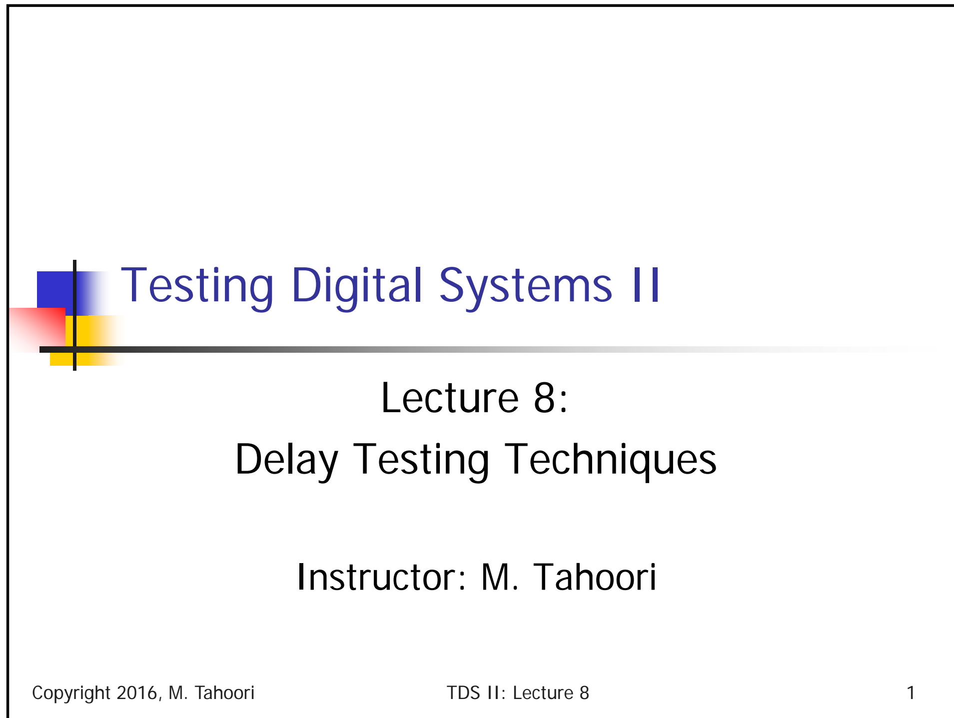
Testing Digital Systems II
Lecture 8:
Delay Testing Techniques
Instructor: M. Tahoori
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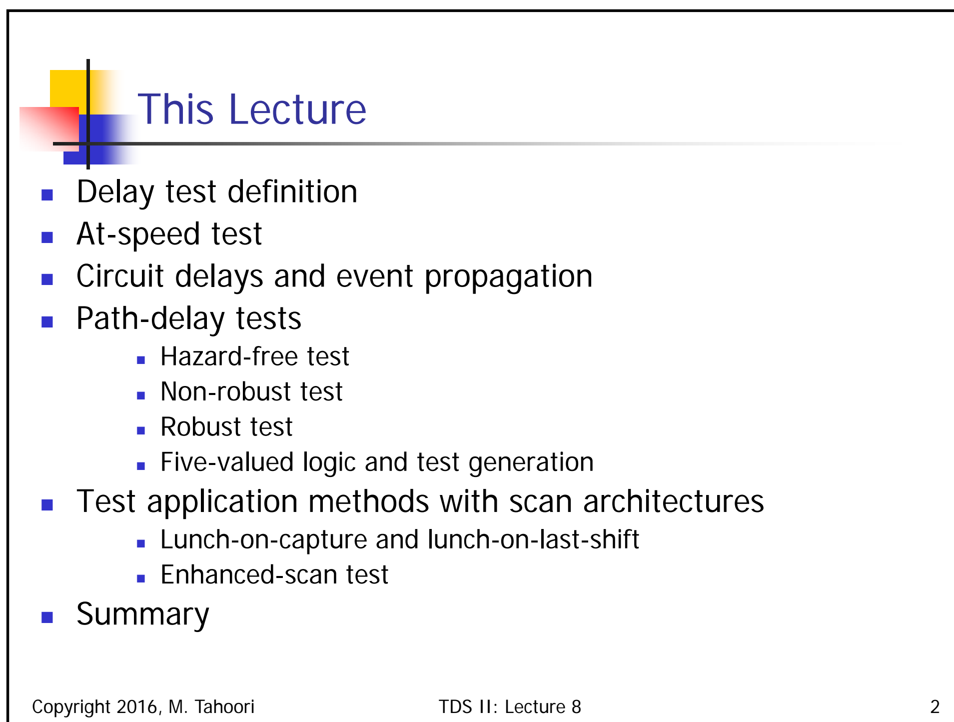
This Lecture
Delay test definition
At-speed test
Circuit delays and event propagation
Path-delay tests
Hazard-free test
Non-robust test
Robust test
Five-valued logic and test generation
Test application methods with scan architectures
Lunch-on-capture and lunch-on-last-shift
Enhanced-scan test
Summary
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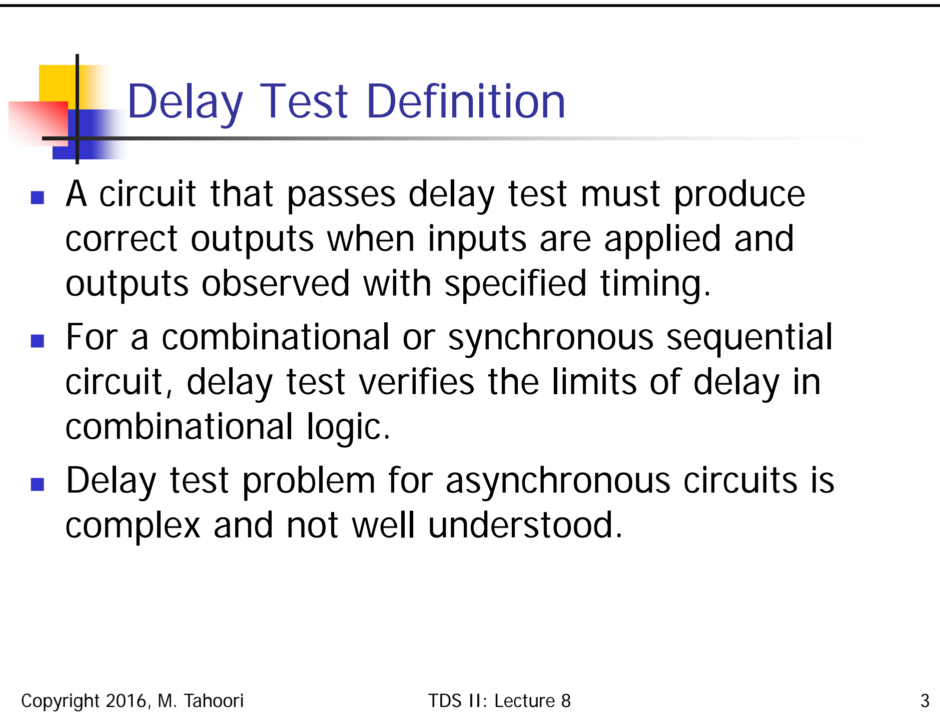
Delay Test Definition
A circuit that passes delay test must produce correct outputs when inputs are applied and outputs observed with specified timing.
For a combinational or synchronous sequential circuit, delay test verifies the limits of delay in combinational logic.
Delay test problem for asynchronous circuits is complex and not well understood.
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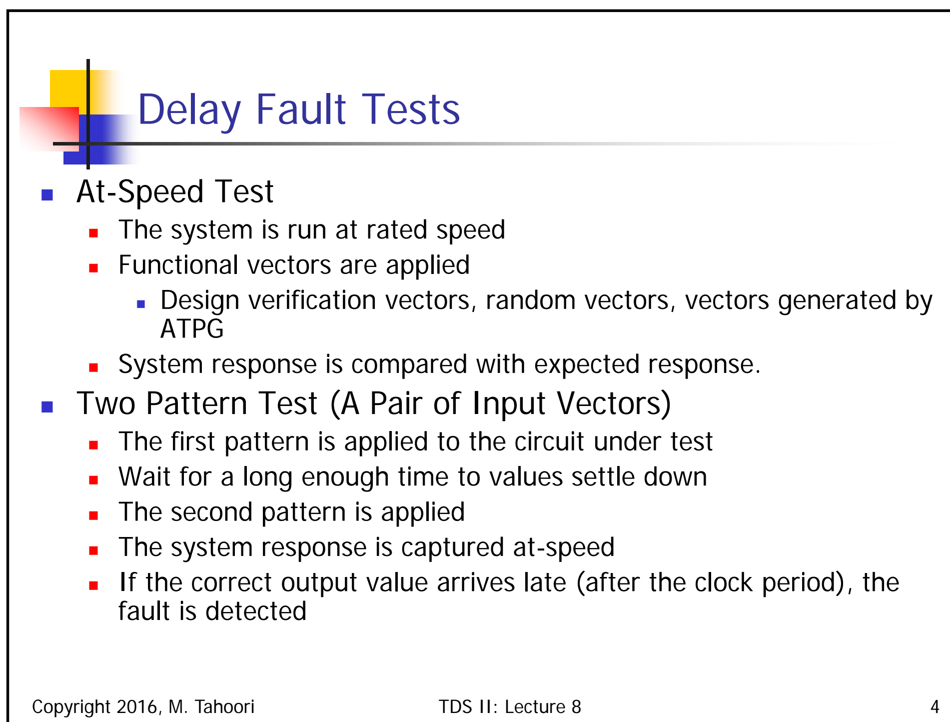
Delay Fault Tests
At-Speed Test
The system is run at rated speed
Functional vectors are applied
Design verification vectors, random vectors, vectors generated by ATPG
System response is compared with expected response.
Two Pattern Test (A Pair of Input Vectors)
The first pattern is applied to the circuit under test
Wait for a long enough time to values settle down
The second pattern is applied
The system response is captured at-speed
If the correct output value arrives late (after the clock period), the fault is detected
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At-Speed Test

- At-speed test means application of test vectors at the rated-clock speed.
- Two methods of at-speed test.
- External test:
  - Vectors may test one or more functional critical (longest delay) paths and a large percentage (~100%) of transition faults.
  - High-speed testers are expensive.
- Built-in self-test (BIST):
  - Hardware-generated random vectors applied to combinational or sequential logic.
  - Only clock is externally supplied.
  - Non-functional paths that are longer than the functional critical path can be activated and cause a good circuit to fail.
  - Some circuits have initialization problem.

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Digital Circuit Timing

Input Signal changes

Output Observation instant

Transient region

Comb. logic

Inputs

Outputs

Synchronized With clock

time

Clock period

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Circuit Delays

- Switching or inertial delay is the interval between input change and output change of a gate:
  - Depends on input capacitance, device (transistor) characteristics and output capacitance of gate.
  - Also depends on input rise or fall times and states of other inputs (second-order effects).
  - Approximation: fixed rise and fall delays (or min-max delay range, or single fixed delay) for gate output.
- Propagation or interconnect delay is the time a transition takes to travel between gates:
  - Depends on transmission line effects (distributed *R*, *L*, *C* parameters, length and loading) of routing paths.
  - Approximation: modeled as lumped delays for gate inputs.

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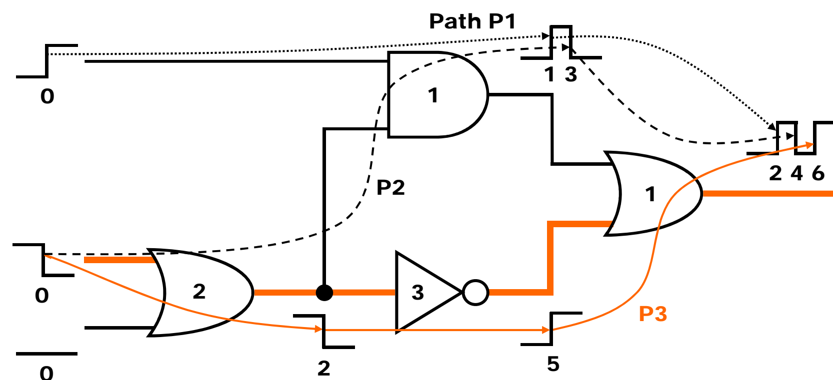
Event Propagation Delays

- Single lumped inertial delay modeled for each gate
  - PI transitions assumed to occur without time skew



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Circuit Outputs

- Each path can potentially produce one signal transition at the output.
- The location of an output transition in time is determined by the delay of the path.

Clock period
Final value
Initial value
Fast transitions
Slow transitions
time
Initial value
Final value

Test Invalidation

- for some delay values a delay fault will not be detected
  - (a) static-0 hazard
  - (b) dynamic hazard

Sample
Fault-free
Fault detected
Test Invalidated
Increasing Delay Fault Size

(a)

Sample
Fault-free
Fault detected
Test Invalidated
Fault detected
Increasing Delay Fault Size

(b)

Hazard-Free Delay Test
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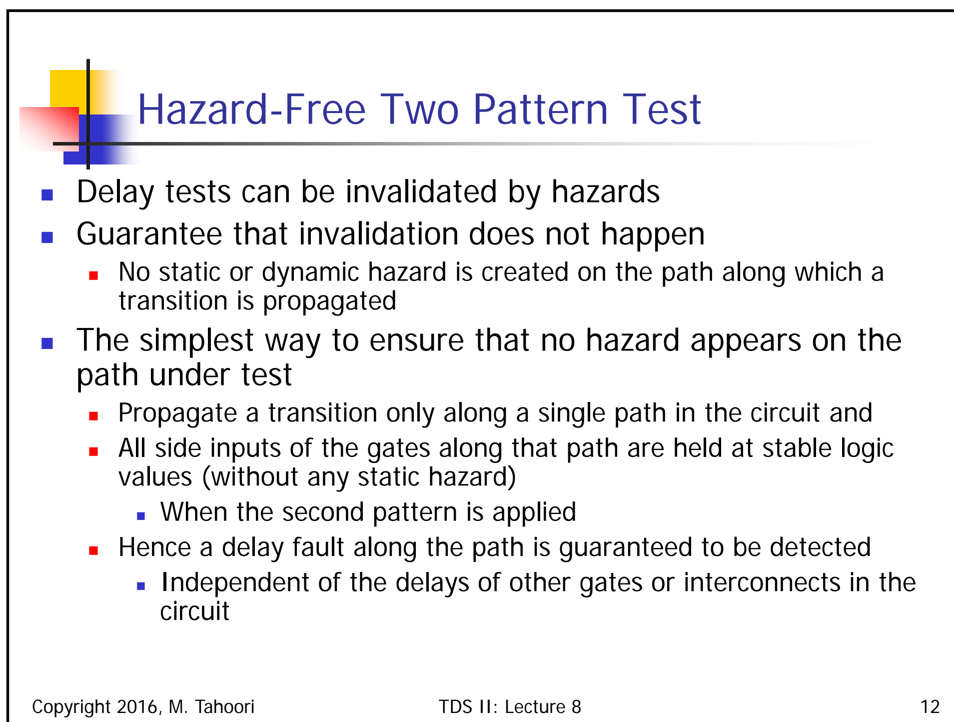
Hazard-Free Two Pattern Test
Delay tests can be invalidated by hazards
Guarantee that invalidation does not happen
No static or dynamic hazard is created on the path along which a transition is propagated
The simplest way to ensure that no hazard appears on the path under test
Propagate a transition only along a single path in the circuit and
All side inputs of the gates along that path are held at stable logic values (without any static hazard)
When the second pattern is applied
Hence a delay fault along the path is guaranteed to be detected
Independent of the delays of other gates or interconnects in the circuit
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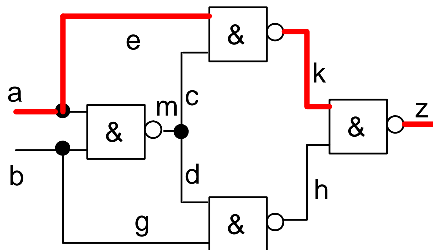
Hazard-Free Two Pattern Test

- Definition:
  - A *hazard-free* test for path *p* is a two pattern delay test where, for all gates lying on *p*, the inputs of the gates not lying on *p* are subject to stable values without any static hazard.
- Example: falling transition along the path a-e-k-z to output z
  - Two patterns: (ab = 10, ab = 00)
    - b stable at 0 ➔ c and h are stable at 1 ➔ hazard-free test



Hazard-Free Two Pattern Test

- If a rising transition along a path is hazard-free testable,
  - The falling transition along that path will also be hazard-free testable, and vice-versa.
- If the two pattern test (v1, v2) is a hazard-free test for a rising transition along a path,
  - The two pattern test (v2, v1) is a hazard-free test for a falling transition along that path
- The sensitization condition for hazard-free testability is very stringent
  - Only very few paths can be tested using hazard-free tests

Hazard-Free Two Pattern Test

- No hazard-free test exists for a transition along the path a-d-h-z

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Robust Test

- 0-to-1 transition along a path from A to Z
  - Hazard-free test: (AB = 01, AB = 11)
  - Robust test: (AB = 0X, AB = 11)
    - B could be 0 in the first pattern
      - Since the logic value on B is non-controlling value during the second pattern,
        - If for some reason the 0-to-1 transition on B arrives late,
        - The 0-to-1 transition at the output Z of the AND gate will be further delayed;
    - There is no chance that the test can get invalidated.

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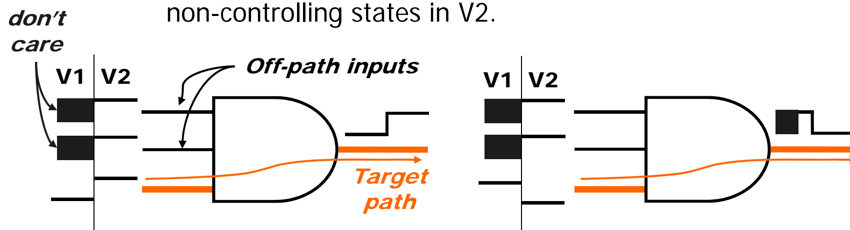
Non-Robust Test

- The delay of a target path is tested if the test propagates a transition via path to a path destination.
- Delay test is a combinational vector-pair, V1,V2, that:
  - Produces a transition at path input.
  - Produces static sensitization -- All off-path inputs assume non-controlling states in V2.



Static sensitization guarantees a test when the target path is the only faulty path. The test is, therefore, called *non-robust.* It is a test with minimal restriction. A path with no such test is a *false path.*

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Robust Test

- A robust test guarantees the detection of a delay fault of the target path, irrespective of delay faults on other paths.
- A robust test is a combinational vector-pair, V1, V2, that satisfies following conditions:
  - Produce *real events* (different steady-state values for V1 and V2) on all on-path signals.
  - All on-path signals must have *controlling events* arriving via the target path.
- A robust test is also a non-robust test.

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Robust Test Conditions

- Real events on target path.
- Controlling events via target path.

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A Five-Valued Algebra

- Signal States: S0, U0 (F0), S1, U1 (R1), XX.
- On-path signals: F0 and R1.
- Off-path signals: F0=U0 and R1=U1.

AND (rows: Input 2; columns: Input 1)

AND	S0	U0	S1	U1	XX
S0	S0	S0	S0	S0	S0
U0	S0	U0	U0	U0	U0
S1	S0	U0	S1	U1	XX
U1	S0	U0	U1	U1	XX
XX	S0	U0	XX	XX	XX

OR (rows: Input 2; columns: Input 1)

OR	S0	U0	S1	U1	XX
S0	S0	U0	S1	U1	XX
U0	U0	U0	S1	U1	XX
S1	S1	S1	S1	S1	S1
U1	U1	U1	S1	U1	U1
XX	XX	XX	S1	U1	XX

NOT

Input	S0	U0	S1	U1	XX
NOT	S1	U1	S0	U0	XX

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Robust Test Generation

Test for ↓P3 – falling transition through path P3: Steps A through E

Non-Robust Test Generation

- Fault ↑P2 – rising transition through path P2 has no robust test.

Applying Two Pattern Tests Using Scan
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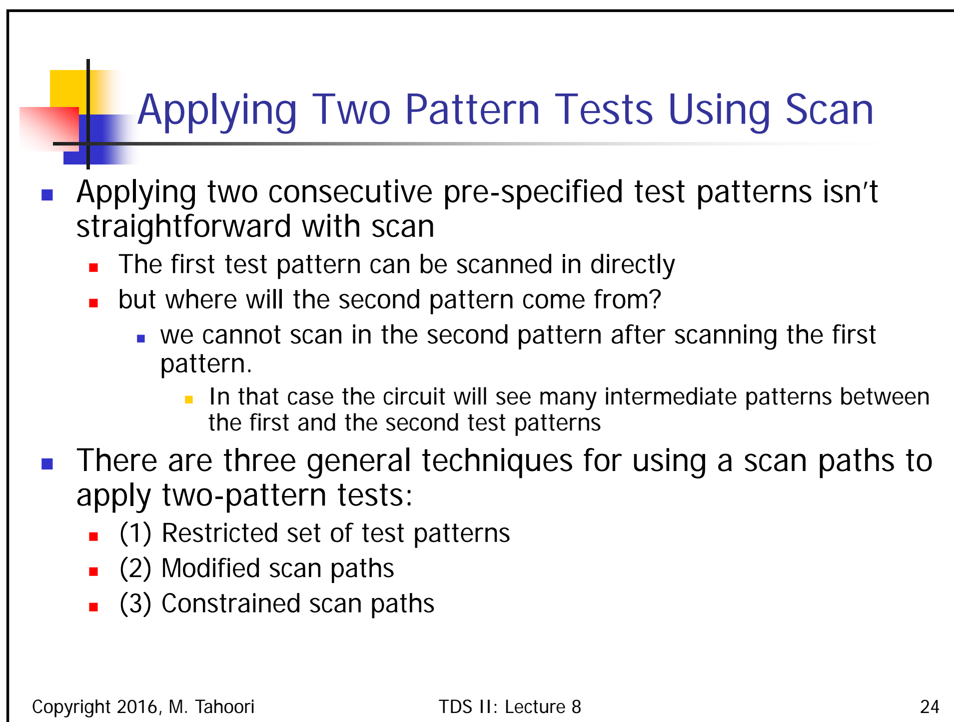
Applying Two Pattern Tests Using Scan
Applying two consecutive pre-specified test patterns isn't straightforward with scan
The first test pattern can be scanned in directly
but where will the second pattern come from?
we cannot scan in the second pattern after scanning the first pattern.
In that case the circuit will see many intermediate patterns between the first and the second test patterns
There are three general techniques for using a scan paths to apply two-pattern tests:
(1) Restricted set of test patterns
(2) Modified scan paths
(3) Constrained scan paths
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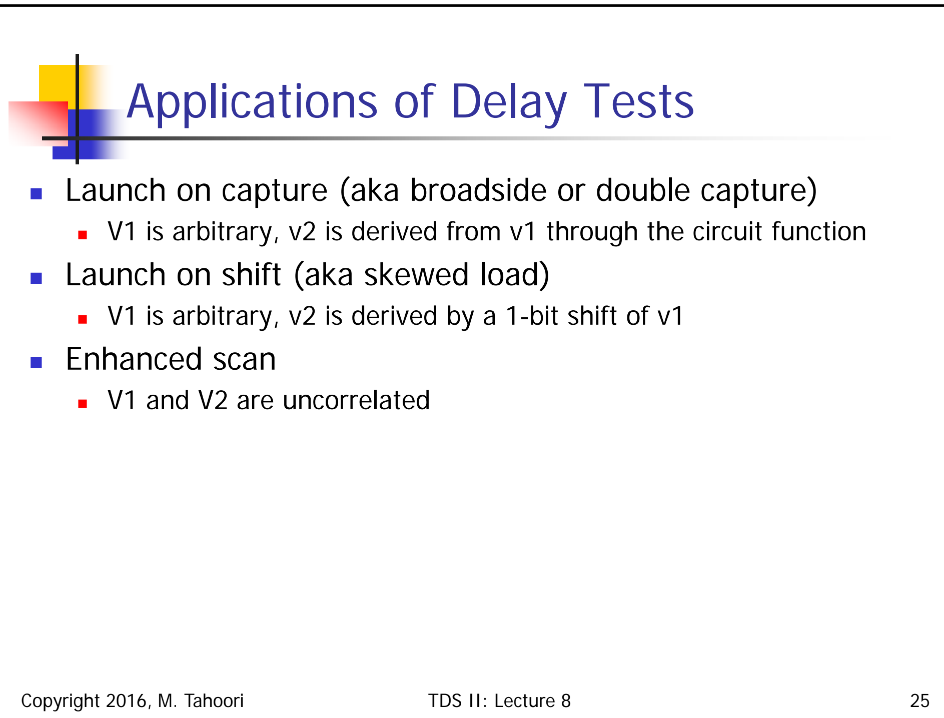
Applications of Delay Tests
Launch on capture (aka broadside or double capture)
V1 is arbitrary, v2 is derived from v1 through the circuit function
Launch on shift (aka skewed load)
V1 is arbitrary, v2 is derived by a 1-bit shift of v1
Enhanced scan
V1 and V2 are uncorrelated
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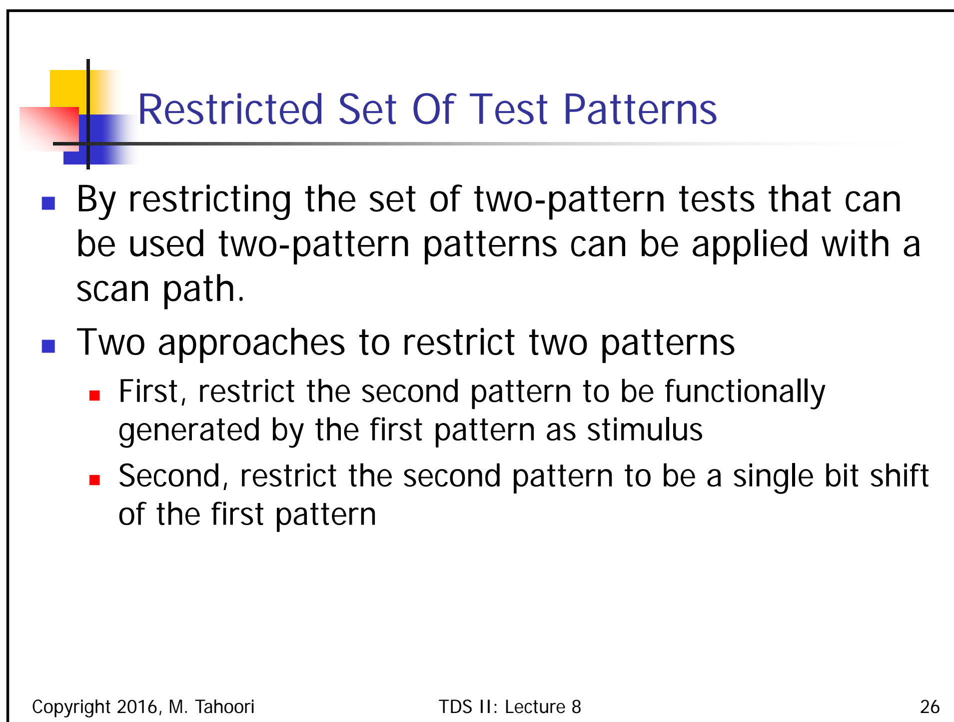
Restricted Set Of Test Patterns
By restricting the set of two-pattern tests that can be used two-pattern patterns can be applied with a scan path.
Two approaches to restrict two patterns
First, restrict the second pattern to be functionally generated by the first pattern as stimulus
Second, restrict the second pattern to be a single bit shift of the first pattern
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Launch On Capture

- Double-pulse delay test (launch-on-capture)
  - The first pattern is scanned into the bistables via the scan path.
  - The second pattern is then loaded from the functional logic outputs into the normal bistable inputs.
    - Any arbitrary first pattern can be scanned in, but the second pattern is greatly restricted based on the functional logic.
    - The second vector can be loaded into the bistables by the application of a single system clock cycle.

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Example: Launch On Capture

- 2-bit binary counter
- Slow-to-rise transition fault at Y
  - Scan-in AB = 00
  - Apply the clock once with T = 0
    - AB = 10
  - Apply the clock again with T = 0
    - Capture the outputs of the combinational logic into the flip-flops
  - Scan out the response
- Cannot test slow-to-fall transition fault on W

Current State	Next State
AB	AB
00	10
10	01
01	11
11	00

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Launch-on-last-shift Delay Test

- Skewed-load delay test (launch-on-last-shift)
  - The second pattern is a single bit shift of the first pattern
    - The first pattern is scanned in
    - The second pattern can be obtained from the first pattern with the application of a single scan clock cycle
      - The set of second patterns is greatly restricted since it must be a shifted version of the first pattern

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Example: Launch-on-last-shift

- Test for a slow-to-fall transition fault on W
  - The second pattern must be AB = 11
  - The first pattern must have B = 0.
    - First scan in AB = 10
    - During the next shift cycle,
      - Apply 1 on SDI
        - Second pattern: AB = 11
- Cannot test for
  - Slow-to-fall transition fault on Z
  - But is testable
    - using the double clocking approach
      - First pattern: AB = 01

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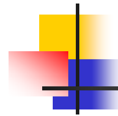
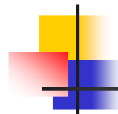


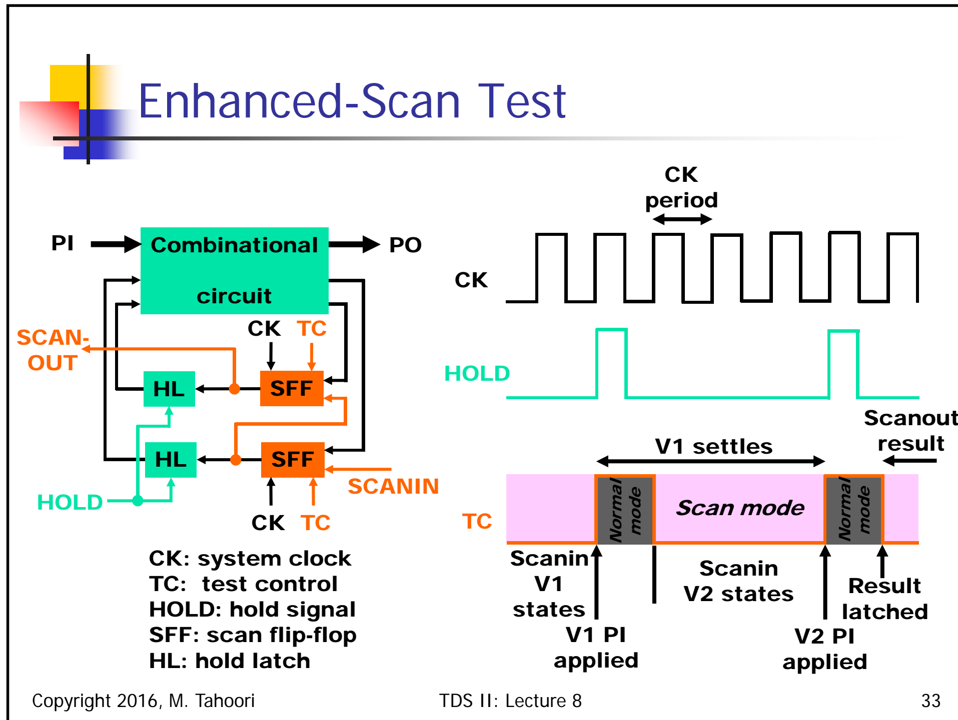
Issues

- Implementation issues of the skewed load technique
  - If the scan path architecture is based on flip-flops, the scan shift is significantly lower speed compared to the system clock
  - Restrictions on the routing of the scan enable signal
    - The scan enable signal should be able to switch from 1-to-0 very quickly
      - After the second pattern appears at the flip-flop outputs, the response of the circuit must be captured within a time equal to the system clock cycle time
  - The above timing problem will not occur in the context of an LSSD-based scan path architecture.



Enhanced-Scan Test

- Any arbitrary vector pairs can be applied
  - Using extra latch per each scan flip-flop
    - HOLD latch
- The first pattern can be scanned in and applied to the functional logic.
- The second pattern can then be scanned in,
  - while the first pattern is still being applied to the functional logic.
- The second pattern can then be applied to the functional logic


Enhanced-Scan Test
PI
Combinational
circuit
PO
SCAN-
OUT
CK
TC
HL
SFF
HL
SFF
SCANIN
HOLD
CK
TC
CK: system clock
TC: test control
HOLD: hold signal
SFF: scan flip-flop
HL: hold latch
CK
period
CK
HOLD
Scanout
result
V1 settles
TC
Normal
mode
Scan mode
Normal
mode
Scanin
V1
states
V1 PI
applied
Scanin
V2 states
V2 PI
applied
Result
latched
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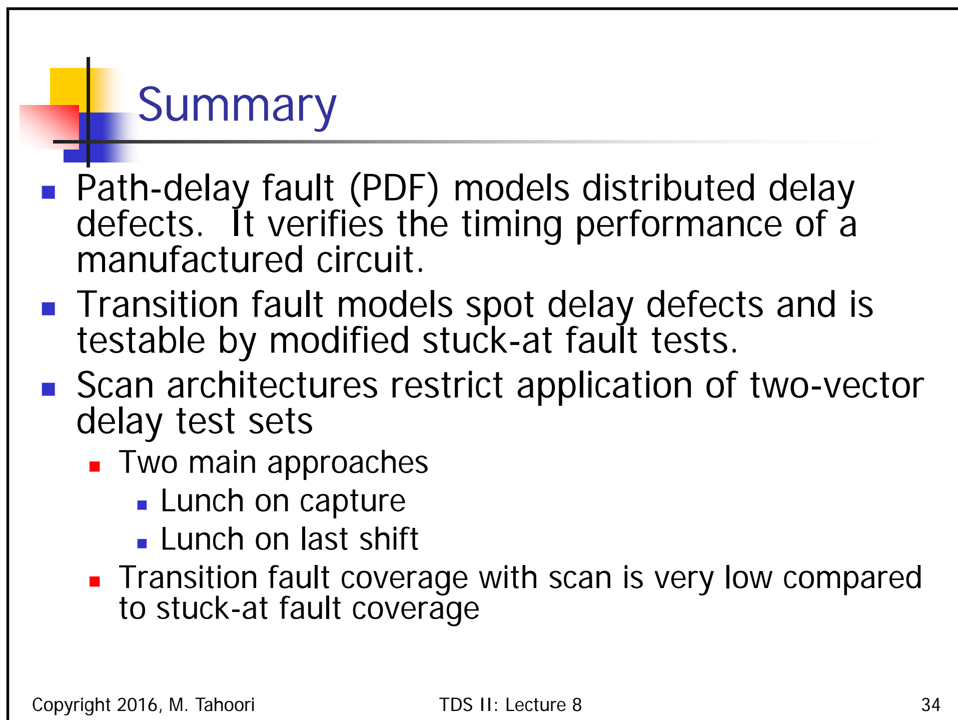
Summary
Path-delay fault (PDF) models distributed delay defects. It verifies the timing performance of a manufactured circuit.
Transition fault models spot delay defects and is testable by modified stuck-at fault tests.
Scan architectures restrict application of two-vector delay test sets
Two main approaches
Lunch on capture
Lunch on last shift
Transition fault coverage with scan is very low compared to stuck-at fault coverage
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