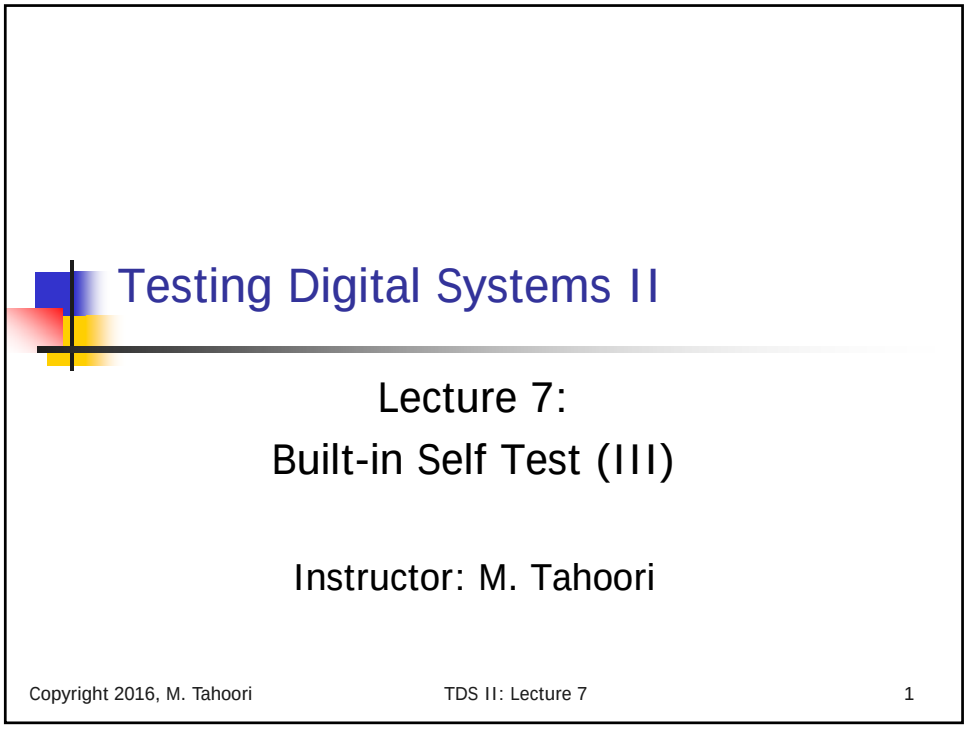
Testing Digital Systems II
Lecture 7:
Built-in Self Test (III)
Instructor: M. Tahoori
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TDS II: Lecture 7
1


BIST Architectures
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TDS II: Lecture 7
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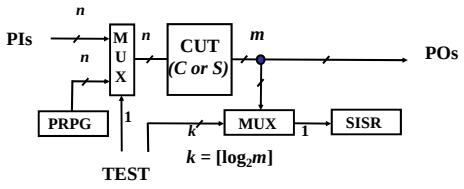
Logic BIST Architectures

Four Types of BIST Architectures:

- No special structure to the CUT
- Make use of scan chains in the CUT
- Configure the scan chains for test pattern generation and output response analysis
- Use concurrent checking circuitry of the design

Centralized and Separate Board-Level BIST (CSBL)

- Two LFSRs and two multiplexers are added to the circuit.
- The first LFSR acts as a PRPG, the second serves as a SISR.
- The first multiplexer selects the inputs, another routes the PO to the SISR.

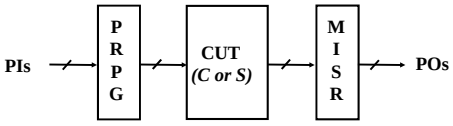


CSBL Architecture

[Benowitz 1975]

Built-In Evaluation and Self-Test (BEST)

- Use a PRPG and a MISR.
- Pseudo-random patterns are applied in parallel from the PRPG to the chip primary inputs (PIs)
- MISR is used to compact the chip output responses

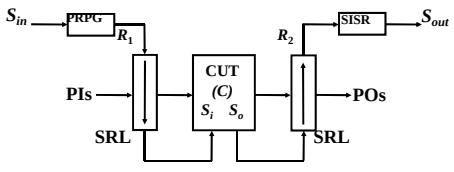


BEST Architecture

[Perkins 1980]

Separate PR-BIST

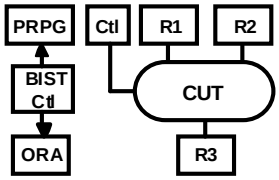
- In addition to the internal scan chain, an external scan chain comprising all primary inputs and primary outputs is required.
- The External scan-chain input is connected to the scan-out point of the internal scan chain.



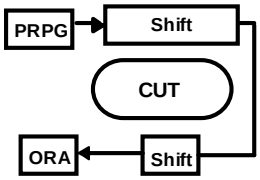
LOCST Architecture

[Eichelberger 1983]

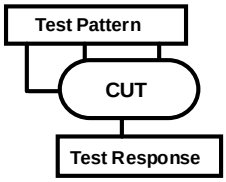
Separate PR-BIST



NORMAL



Shift Test Pattern In, Response Out

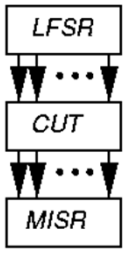


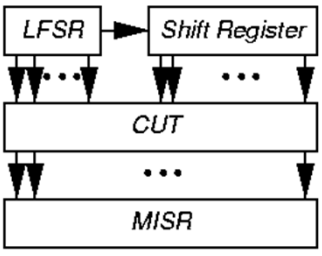
Apply Pattern, Get Response

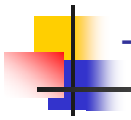
- Drawbacks: Long Test Time, Poor Delay Fault Cover
- Advantages: Low Overhead, Simple Control Logic

Test-per-Clock System

- New fault set tested every clock period
- Shortest possible pattern length
  - 10 million BIST vectors, 200 MHz test / clock
  - Test Time = 10,000,000 / 200 x 10^6 = 0.05 s







Test-per-Scan System

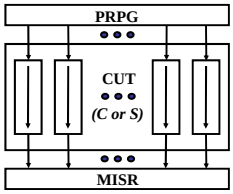
- New fault tested during 1 clock vector with a complete scan chain shift
- More time required per test than test-per-clock
  - Advantage:
    - Combination of scan chains and MISR reduces MISR bit width
  - Disadvantage:
    - Much longer test pattern set length, causes fault simulation problems
- Input patterns – time shifted & repeated
  - Become correlated – reduces fault detection effectiveness
  - Use XOR network to phase shift & decorrelate

STUMPS

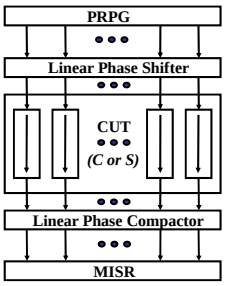
- **S**elf-**T**est **U**sing **M**ISR and **P**arallel **S**hift register sequence generator
- Originally proposed to reduce overhead of LFSR/MISR for application to testing multi-chip boards, each of which has only the Shift Registers
- Can also be used on a single chip with multiple scan chains

STUMPS Example

- SR1 ... SRn – 25 full-scan chains, each 200 bits
- 5000 chip outputs, need 25 bit MISR (not 5000 bits)



STUMPS



A STUMPS-based Architecture

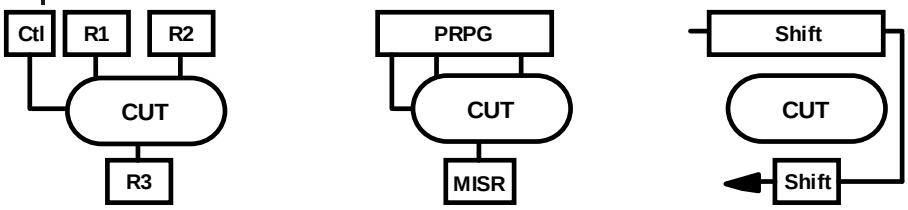
STUMPS

- Test procedure:
  - Scan in patterns from LFSR into all scan chains (200 clocks)
  - Switch to normal functional mode and clock 1 x with system clock
  - Scan out chains into MISR (200 clocks) where test results are compacted
    - Overlap Steps 1 & 3
- Requirements:
  - Every system input is driven by a scan chain
  - Every system output is caught in a scan chain or drives another chip being sampled

Built-In Logic Block Observer (BILBO)

- The architecture applies to circuits that can be partitioned into independent modules (logic blocks).
- Each module is assumed to have its own input and output registers (storage elements)
  - Or such registers are added to the circuit where necessary.
- The registers are redesigned so that for test purposes they act as PRPGs or MISRs.

Embedded PR-BIST —BILBO



NORMAL

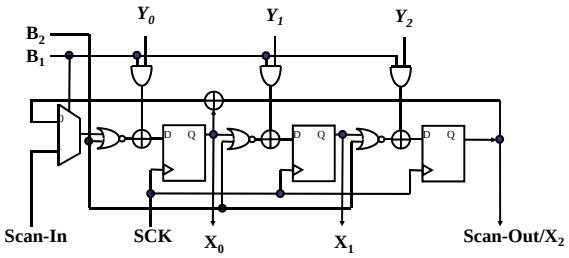
Apply Test,
Compact Response

Shift
Signature Out

- Drawbacks: Multiple Test Sessions, Complex Control
  - Register Self-adjacency Concerns
- Advantages: At-speed Test, Reuse System Bistables

Built-In Logic Block Observer

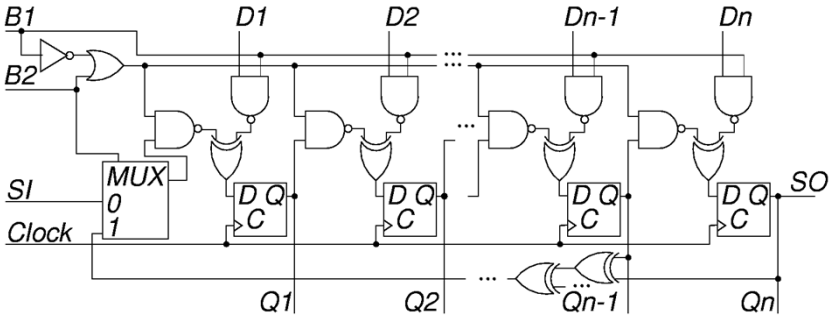
B_1	B_2	Operation mode
1	1	Normal
0	0	Scan
1	0	Mixed Test Generation and Signature Analysis
0	1	Reset



A 3-stage BILBO

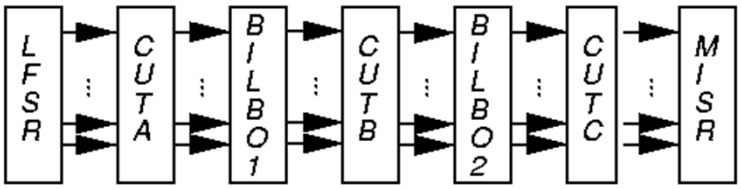
Another BILBO Register

- B1 and B2 configure as
  - **Shift register** for scan (B1B2= 00),
  - **LFSR** (B1B2 = 01),
  - **MISR** (B1B2 = 11)
  - **Normal** (B1B2 = 10)



Example BILBO Usage

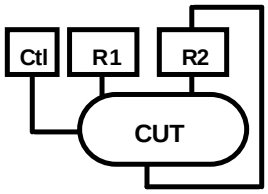
- SI – Scan In
- SO – Scan Out
- Characteristic polynomial: $1 + x + ... + x^n$
- CUTs A and C: BILBO1 is MISR, BILBO2 is LFSR
- CUT B: BILBO1 is LFSR, BILBO2 is MISR



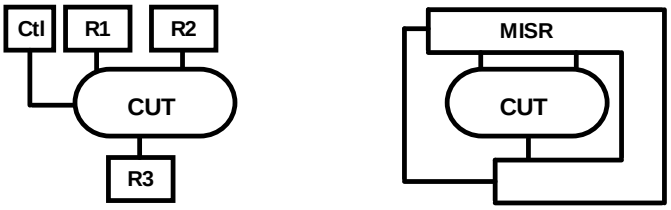
(a) Example test configuration.

Register self-Adjacency

- Register *R2* is self-adjacent
  - It should act as LFSR and MISR at the same time
  - Cannot use BILBO register



Embedded PR-BIST —Circular

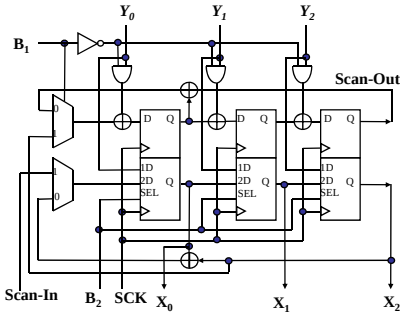


Normal Test

- Drawbacks: Scan Dependence Concerns
- Advantages: At-speed Test, Reuse System Bistables
  - Simple Control Logic, Short Test Time

Concurrent Built-In Logic Block Observer (CBILBO)

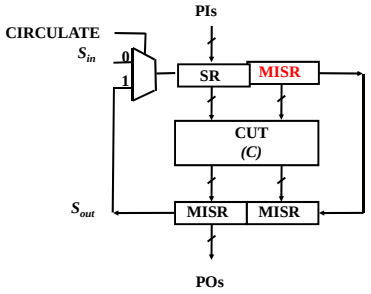
B_1	B_2	Operation mode
-	0	Normal
1	1	Scan
0	1	Test Generation and Signature Analysis



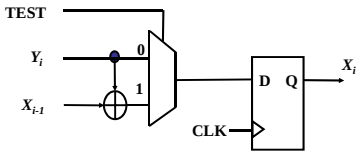
[Wang 1986c]

A 3-stage concurrent BILBO (CBILBO)

Circular Self-Test Path



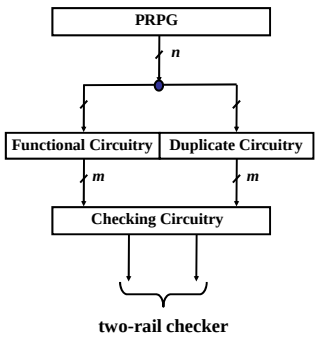
(a) The CSTP architecture



(b) Self-Test cell

CSTP architecture

Concurrent Self-Verification (CSV)



CSV Architecture

Summary

Architecture	*Level*	*TPG*	*ORA*	*Circuit*	*BIST*
CSBL	B or C	PRPG	SISR	C or S	Test-Per-Clock
BEST	B or C	PRPG	MISR	C or S	Test-Per-Clock
LOCST	C	PRPG	SISR	C	Test-Per-Scan
STUMPS	B or C	PRPG	MISR	C	Test-Per-Scan
BILBO	C	PRPG	MISR	C	Test-Per-Clock
CBILBO	C	EPG/PEPG	MISR	C	Test-Per-Clock
CSTP	C	PRPG	MISR	C or S	Test-Per-Clock
CSV	C	PRPG	Checker	C or S	Test-Per-Clock

B: board-level testing
C: combinational circuit
S: sequential circuit

Representative Logic BIST Architectures