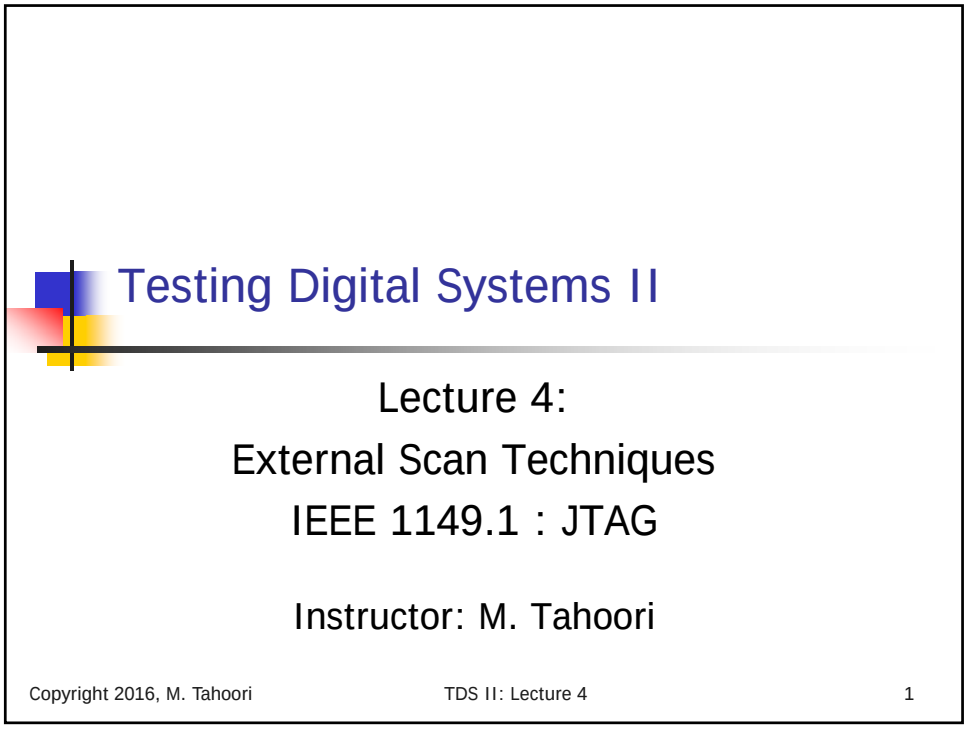
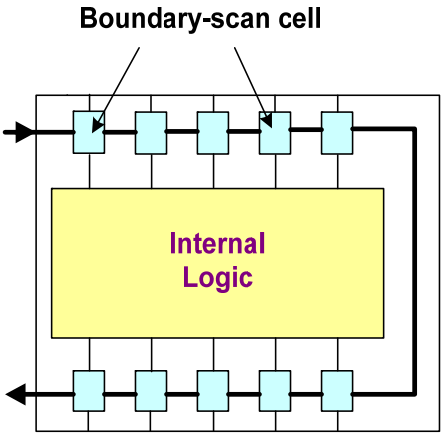


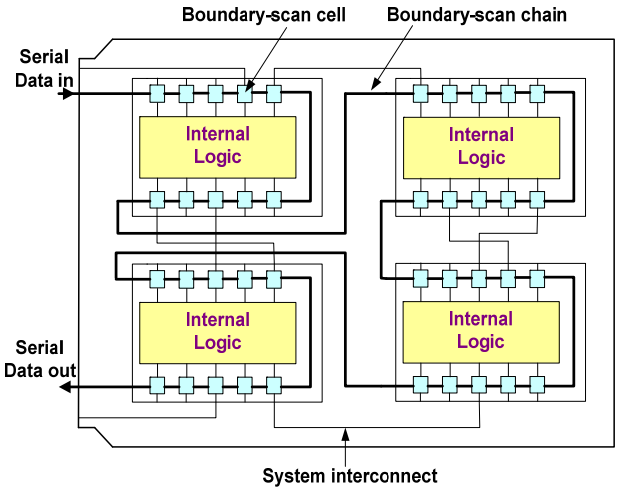
Purpose of Standard

- Originally a DFT technique for PCBs
- Lets test instructions and test data be serially fed into a *component-under-test* (CUT)
  - Allows reading out of test results
- JTAG can operate at chip, PCB, and system levels
- Allows control of tri-state signals during testing
- Lets other chips collect responses from CUT
- Lets system interconnect be tested separately from components
- Lets components be tested separately from wires

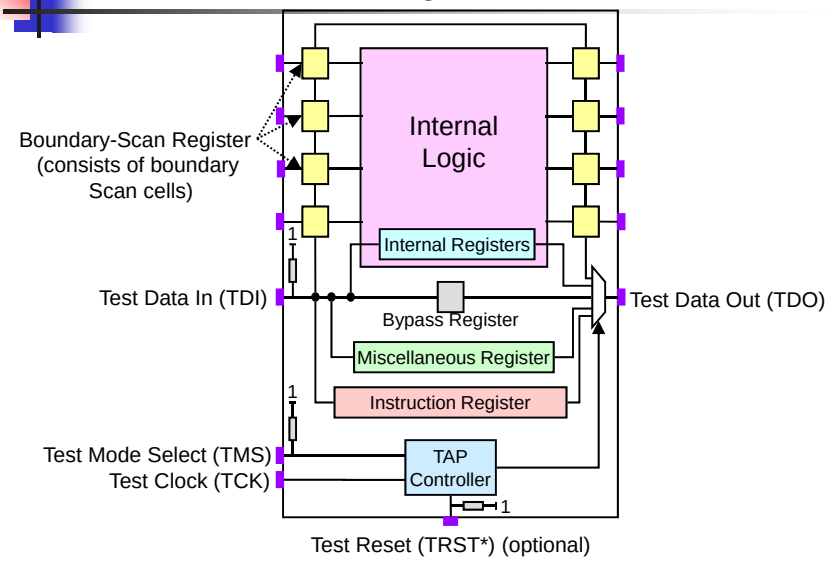
Basic Idea of Boundary Scan



A Board Containing 4 IC's with Boundary Scan



1149.1 Boundary-Scan Architecture



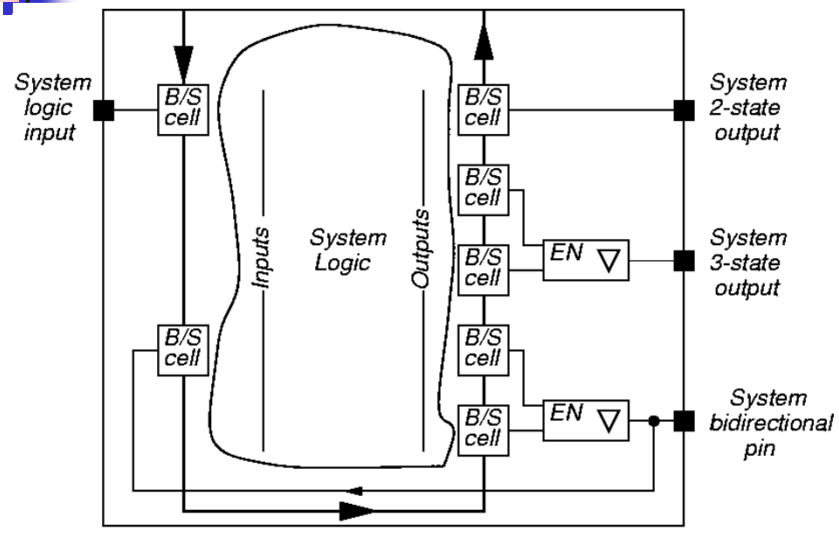
Hardware Components of 1149.1

- A test access port (TAP) consisting of :
  - 4 mandatory pins: Test data in (TDI), Test data out (TDO), Test mode select (TMS), Test clock (TCK), and
  - 1 optional pin: Test reset (TRST)
- A test access port controller (TAPC)
- An instruction register (IR)
- Several test data registers
  - A boundary scan register (BSR) consisting of boundary scan cells (BSCs)
  - A bypass register (BR)
  - Some optional registers
    - Device-ID register, design-specified registers such as scan registers, LFSRs for BIST, etc.

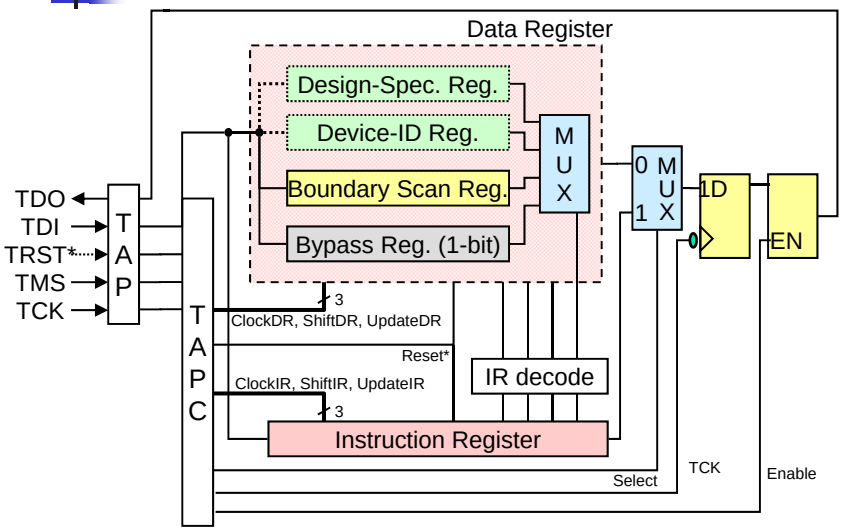
Basic Operations

1. Instruction sent (serially) through TDI into instruction register.
2. Selected test circuitry configured to respond to the instruction.
3. Test pattern shifted into selected data register and applied to logic to be tested
4. Test response captured into some data register
5. Captured response shifted out; new test pattern shifted in simultaneously
6. Steps 3-5 repeated until all test patterns are applied.

System View of Interconnect



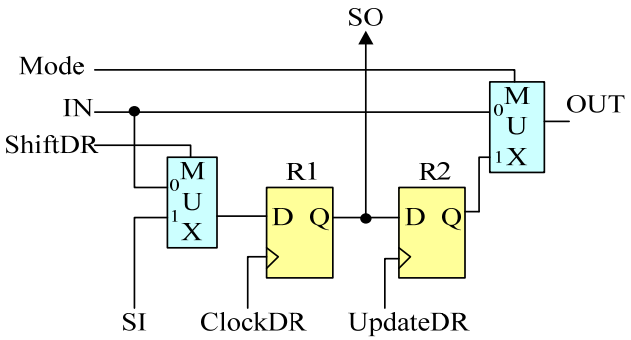
Boundary-Scan Circuitry in A Chip



Data registers

- Boundary scan register: consists of boundary scan cells
- Bypass register: a one-bit register used to pass test signal from a chip when it is not involved in current test operation
- Device-ID register: for the loading of product information (manufacturer, part number, version number, etc.)
- Other user-specified data registers (scan chains, LFSR for BIST, etc.)

A Typical Boundary-Scan Cell (BSC)

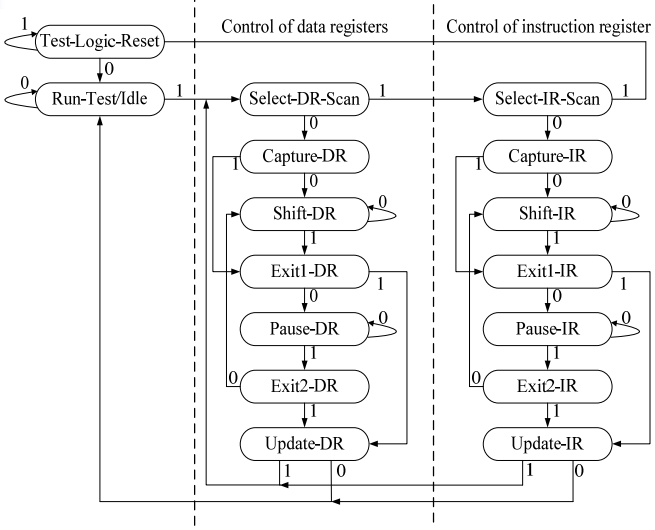


- Operation modes
  - Normal: IN → OUT (Mode = 0)
  - Shift: TDI → ... → IN → OUT → ... → TDO (ShiftDR = 1, ClockDR)
  - Capture: IN → R1, OUT driven by IN or R2 (ShiftDR = 0, ClcokDR)
  - Update: R1 → OUT (Mode_Control = 1, UpdateDR)

TAP Controller

- A finite state machine with 16 states
- Input: TCK, TMS
- Output: 9 or 10 signals included ClockDR, UpdateDR, ShiftDR, ClockIR, UpdateIR, ShiftIR, Select, Enable, TCK and TRST* (optional).

State Diagram of TAP Controller



Main functions of TAP controller

- Providing control signals to
  - Reset BS circuitry
  - Load instructions into instruction register
  - Perform test capture operation
  - Perform test update operation
  - Shift test data in and out

States of TAP Controller

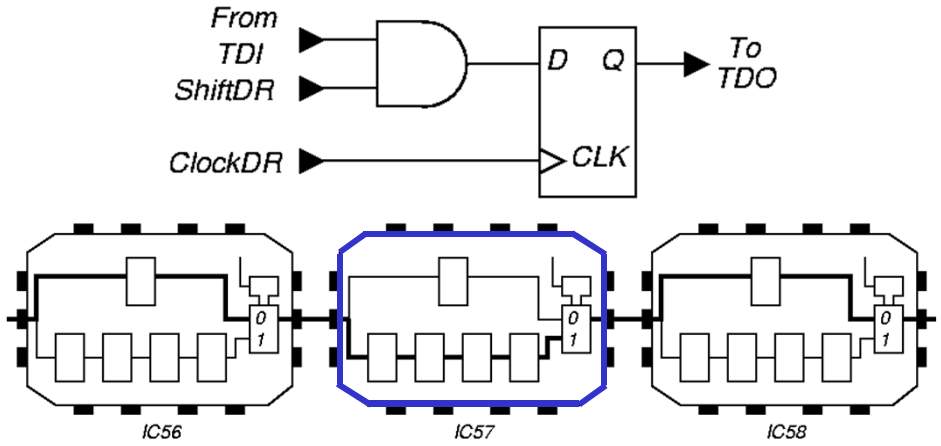
- Test-Logic-Reset: normal mode
- Run-Test/Idle: wait for internal test such as BIST
- Select-DR-Scan: initiate a data-scan sequence
- Capture-DR: load test data in parallel
- Shift-DR: load test data in series
- Exit1-DR: finish phase-1 shifting of data
- Pause-DR: temporarily hold the scan operation (e.g., allow the bus master to reload data)
- Exit2-DR: finish phase-2 shifting of data
- Update-DR: parallel load from associated shift registers
- Note: Controls for IR are similar to those for DR.

Instruction Set

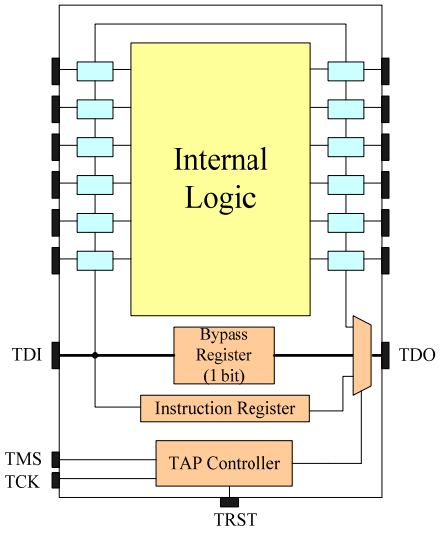
- BYPASS
  - Bypass data through a chip
- SAMPLE
  - Sample (capture) test data into BSR
- PRELOAD
  - Shift-in test data and update BSR
- EXTEST
  - Test interconnection between chips of board
- Optional
  - INTEST, RUNBIST, CLAMP, IDCODE, USERCODE, HIGH-Z, etc.

BYPASS Instruction

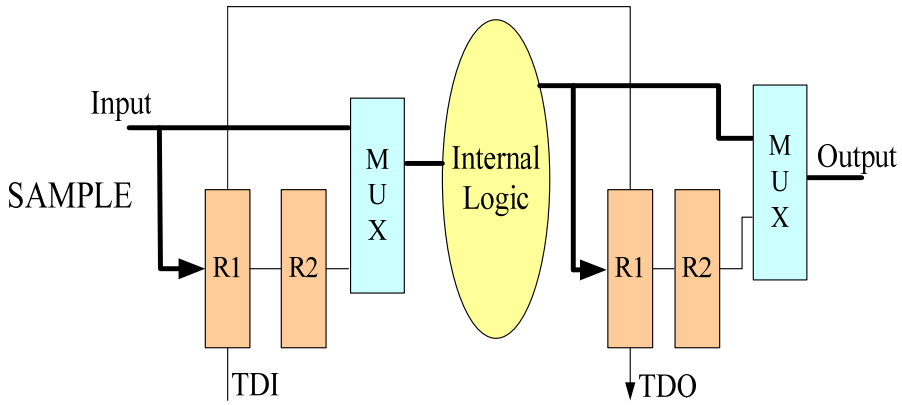
- Purpose: Bypasses scan chain with 1-bit register



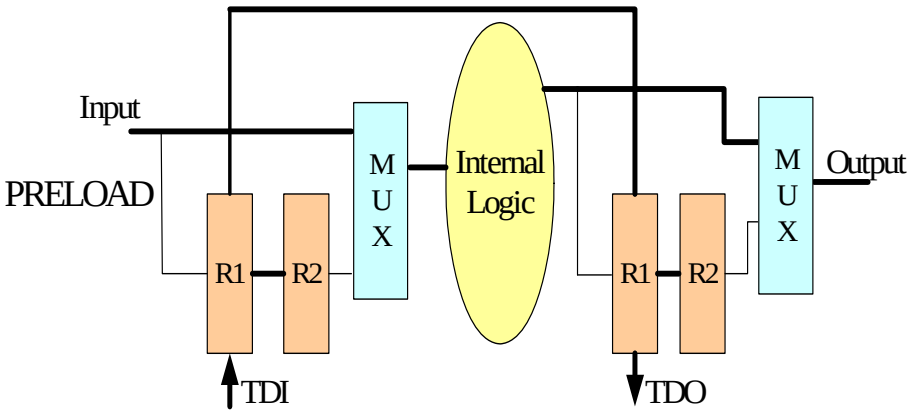
Execution of BYPASS Instruction



Execution of SAMPLE Instruction

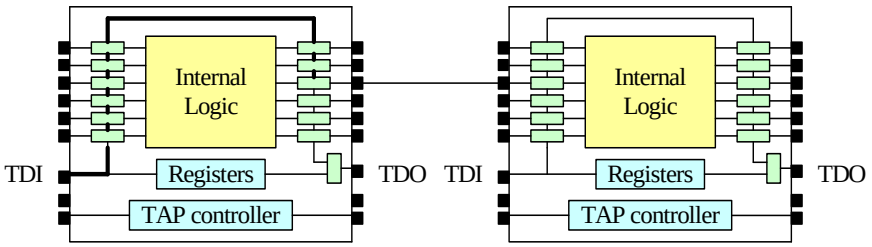


Execution of PRELOAD Instruction



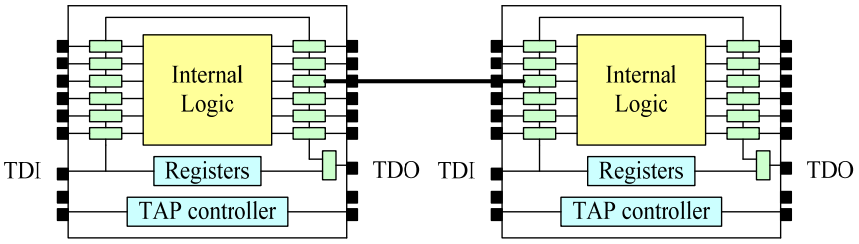
Execution of EXTEST Instruction (1/3)

- Shift-DR (Chip1)



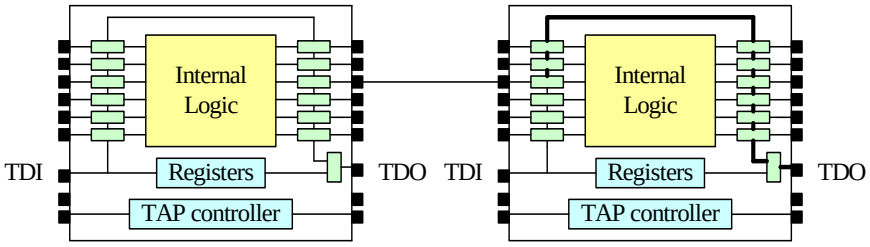
Execution of EXTEST Instruction (2/3)

- Update-DR (Chip1)
- Capture-DR (Chip2)



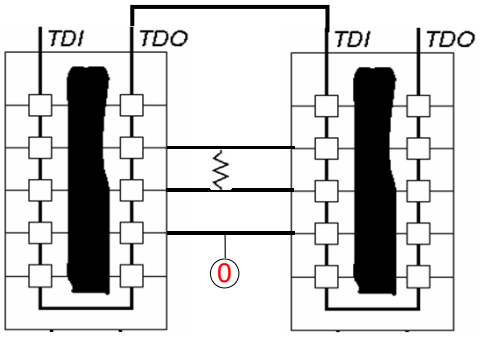
Execution of EXTEST Instruction (3/3)

- Shift-DR (Chip2)



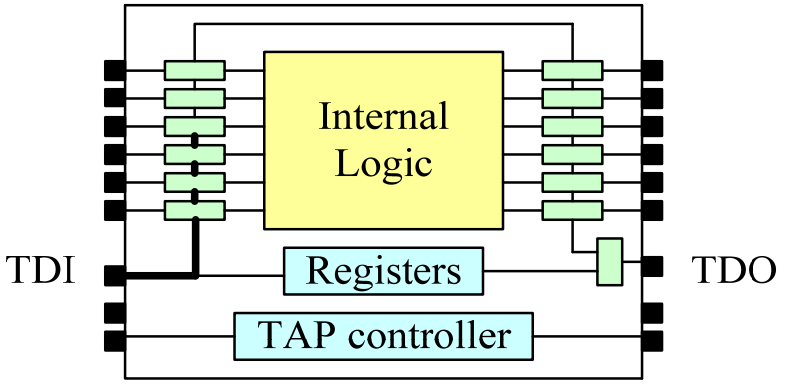
External Test

- Example of testing interconnects
  - Input: X X X X X X **1 0 1** X X X X X X X X X X
  - Output: X X X X X X X X X X X **0** **0** **0** X X X X X



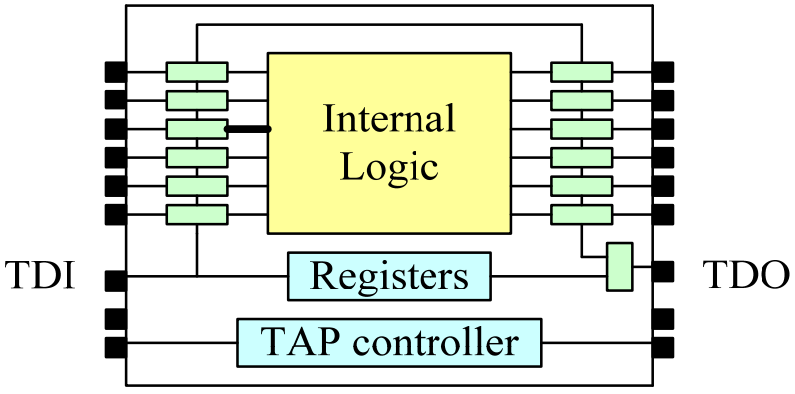
Execution of INTEST Instruction (1/4)

- Shift-DR



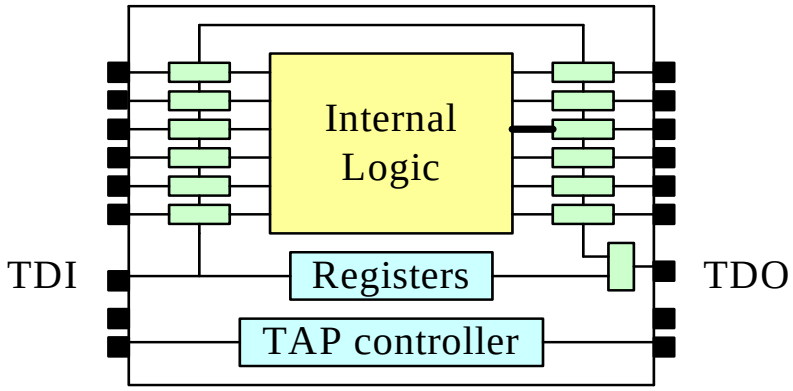
Execution of INTEST Instruction (2/4)

- Update-DR



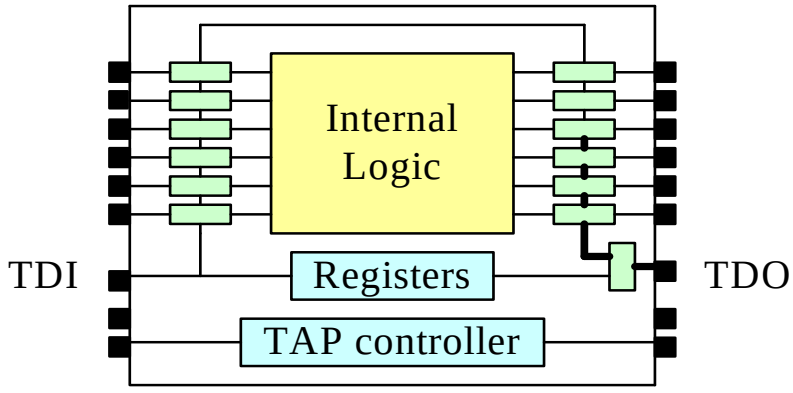
Execution of INTEST Instruction (3/4)

- Capture-DR



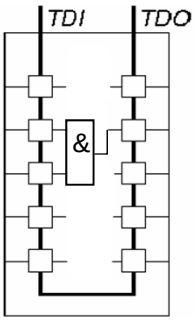
Execution of INTEST Instruction (4/4)

- Shift-DR



Internal Test

- Example of testing chip logic
  - Input: X 1 0 X X X X X X X
  - Good output: X 0 X X X X X X X X

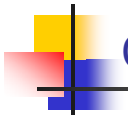


RUNBIST Instruction

- Purpose:
  - Allows to issue BIST command to component through JTAG hardware
- Optional instruction
- Lets test logic control state of output pins
  - Can be determined by pin boundary scan cell
  - Can be forced into high impedance state
- BIST result (success or failure) can be left in boundary scan cell or internal cell
  - Shift out through boundary scan chain
- May leave chip pins in an indeterminate state (reset required before normal operation resumes)

IDCODE Instruction

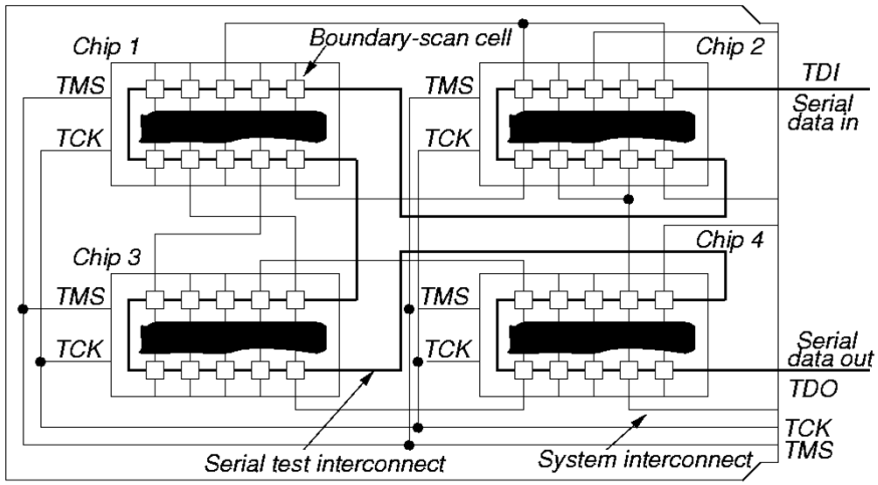
- Purpose: Connects the component device identification register serially between *TDI* and *TDO*
  - In the *Shift-DR* TAP controller state
- Allows board-level test controller or external tester to read out component ID
- Required whenever a JEDEC identification register is included in the design



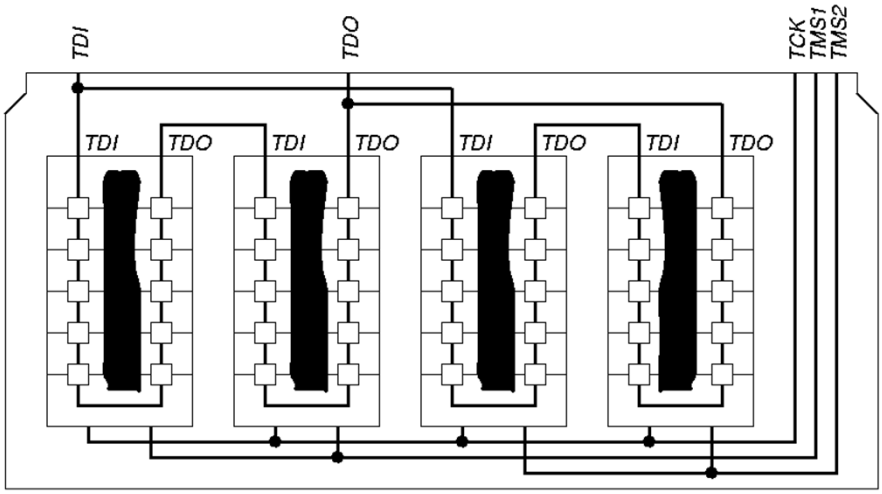
Optional / Required Instructions

Instruction	Status
BYPASS	Mandatory
CLAMP	Optional
EXTEST	Mandatory
HIGHZ	Optional
IDCODE	Optional
INTEST	Optional
RUNBIST	Optional
SAMPLE/PRELOAD	Mandatory
USERCODE	Optional

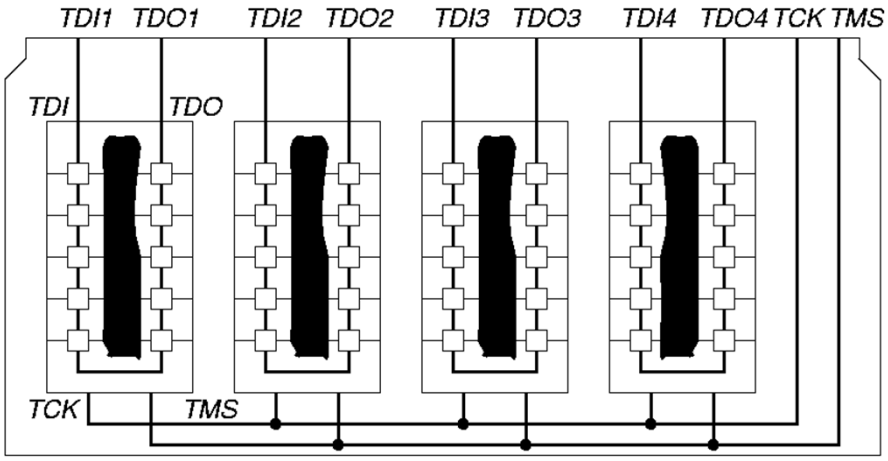
Serial Board / MCM Scan



Parallel Board / MCM Scan



Independent Path Board / MCM Scan



Summary

- Boundary Scan Standard has become absolutely essential
  - No longer possible to test printed circuit boards with *bed-of-nails* tester
  - Not possible to test multi-chip modules at all without it
  - Supports BIST, external testing with Automatic Test Equipment, and boundary scan chain reconfiguration as BIST pattern generator and response compacter
  - Now getting widespread usage