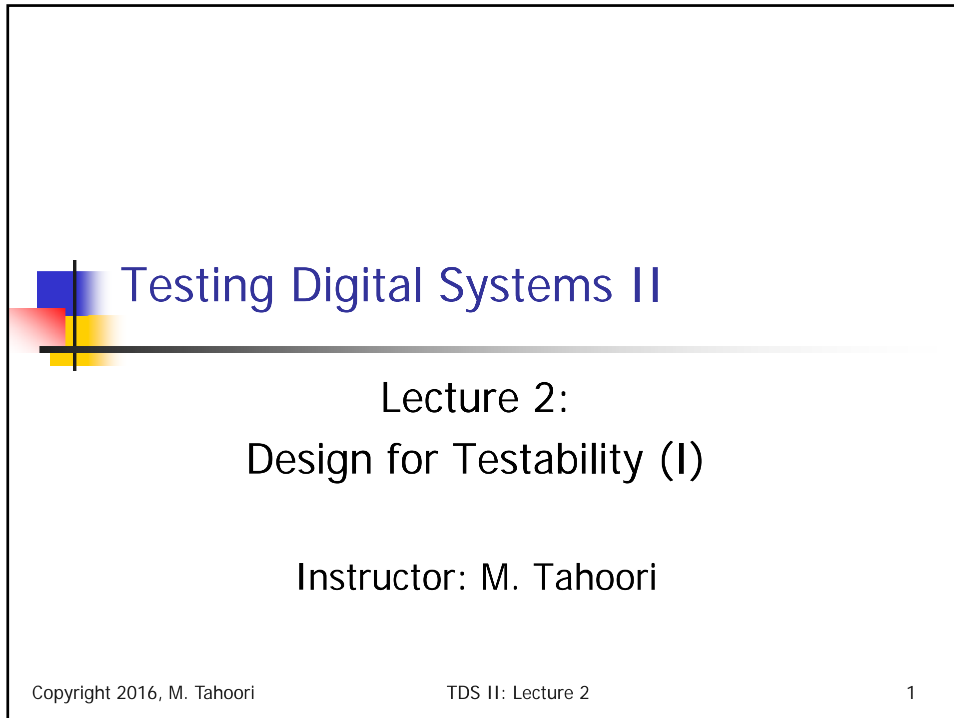
Testing Digital Systems II
Lecture 2:
Design for Testability (I)
Instructor: M. Tahoori
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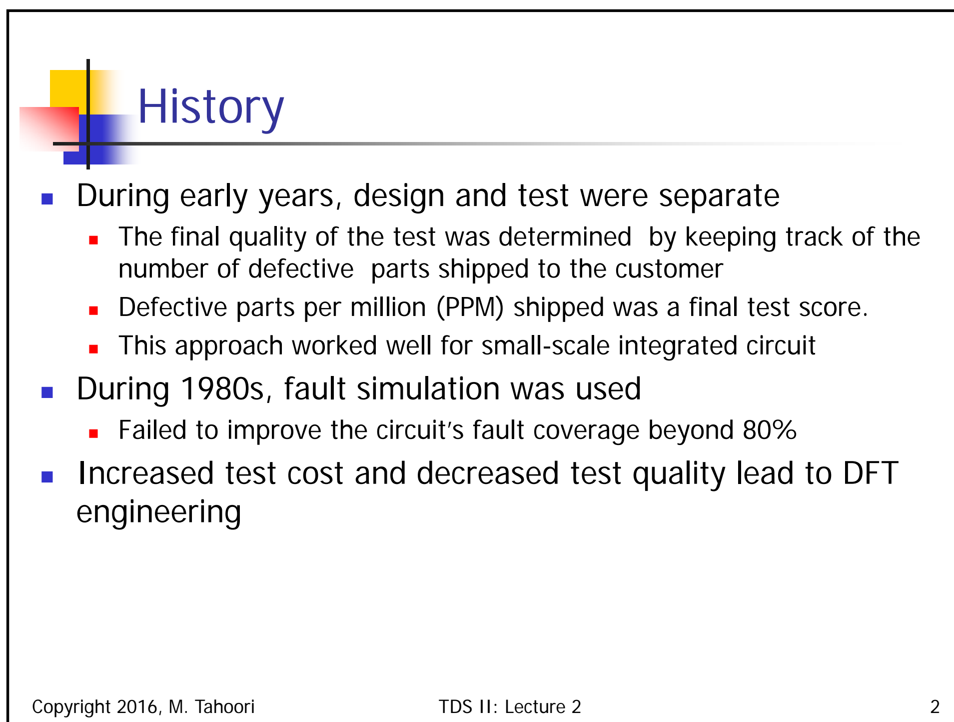
History
During early years, design and test were separate
The final quality of the test was determined by keeping track of the number of defective parts shipped to the customer
Defective parts per million (PPM) shipped was a final test score.
This approach worked well for small-scale integrated circuit
During 1980s, fault simulation was used
Failed to improve the circuit's fault coverage beyond 80%
Increased test cost and decreased test quality lead to DFT engineering
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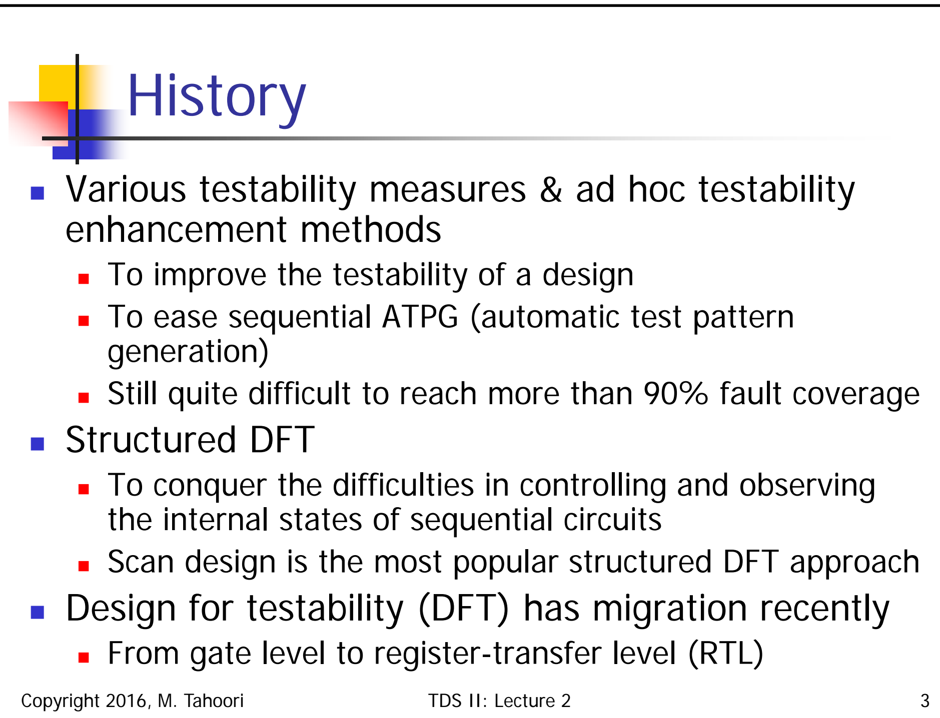
History
Various testability measures & ad hoc testability enhancement methods
To improve the testability of a design
To ease sequential ATPG (automatic test pattern generation)
Still quite difficult to reach more than 90% fault coverage
Structured DFT
To conquer the difficulties in controlling and observing the internal states of sequential circuits
Scan design is the most popular structured DFT approach
Design for testability (DFT) has migration recently
From gate level to register-transfer level (RTL)
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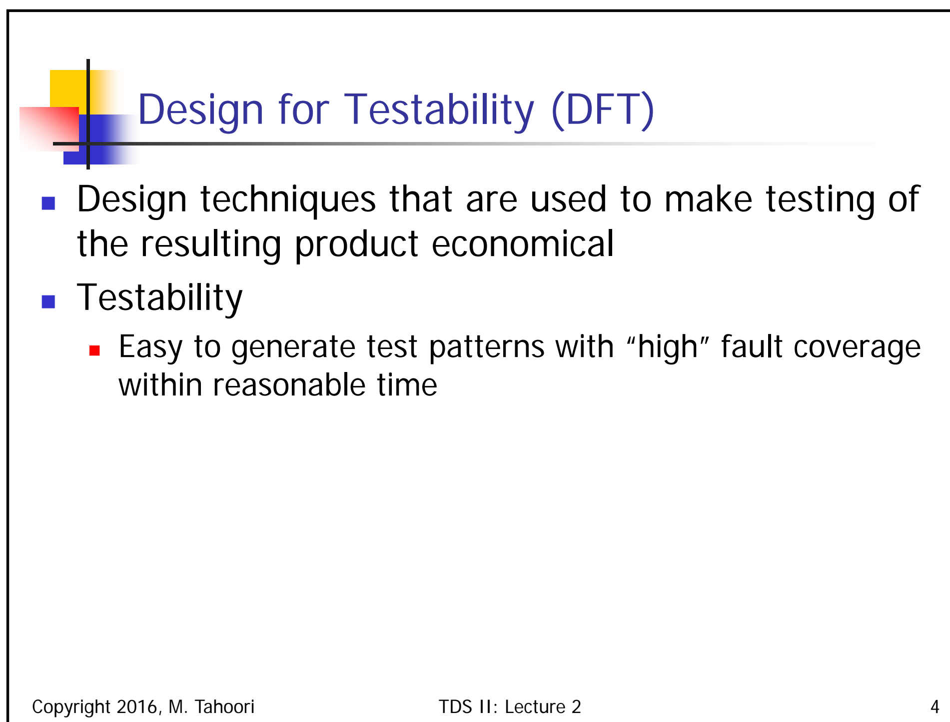
Design for Testability (DFT)
Design techniques that are used to make testing of the resulting product economical
Testability
Easy to generate test patterns with "high" fault coverage within reasonable time
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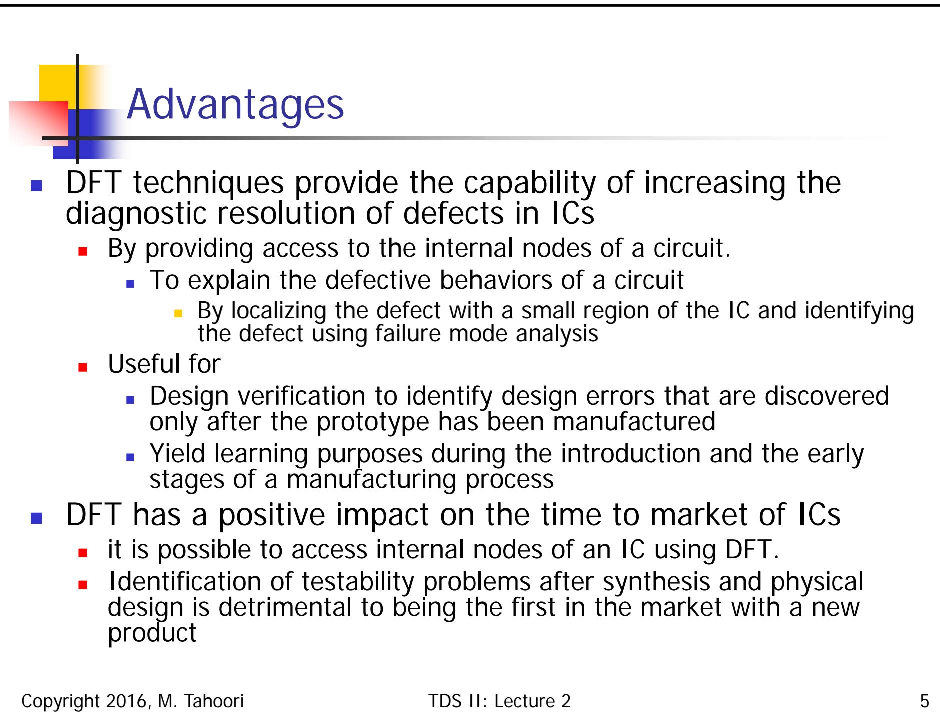

Advantages
- DFT techniques provide the capability of increasing the diagnostic resolution of defects in ICs
  - By providing access to the internal nodes of a circuit.
    - To explain the defective behaviors of a circuit
      - By localizing the defect with a small region of the IC and identifying the defect using failure mode analysis
  - Useful for
    - Design verification to identify design errors that are discovered only after the prototype has been manufactured
    - Yield learning purposes during the introduction and the early stages of a manufacturing process
- DFT has a positive impact on the time to market of ICs
  - it is possible to access internal nodes of an IC using DFT.
  - Identification of testability problems after synthesis and physical design is detrimental to being the first in the market with a new product
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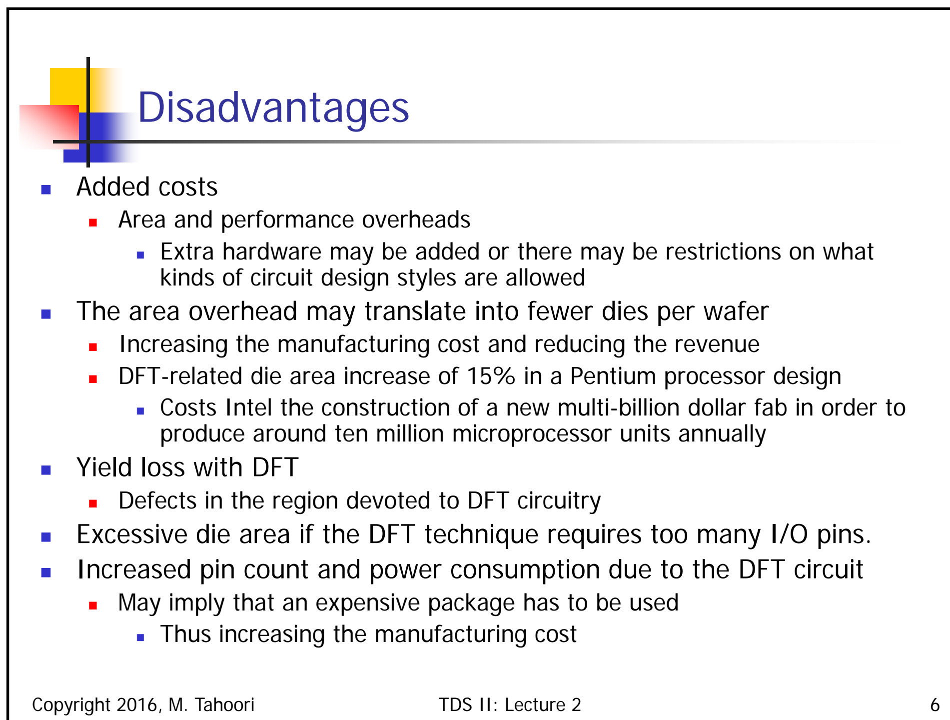

Disadvantages
- Added costs
  - Area and performance overheads
    - Extra hardware may be added or there may be restrictions on what kinds of circuit design styles are allowed
- The area overhead may translate into fewer dies per wafer
  - Increasing the manufacturing cost and reducing the revenue
  - DFT-related die area increase of 15% in a Pentium processor design
    - Costs Intel the construction of a new multi-billion dollar fab in order to produce around ten million microprocessor units annually
- Yield loss with DFT
  - Defects in the region devoted to DFT circuitry
- Excessive die area if the DFT technique requires too many I/O pins.
- Increased pin count and power consumption due to the DFT circuit
  - May imply that an expensive package has to be used
    - Thus increasing the manufacturing cost
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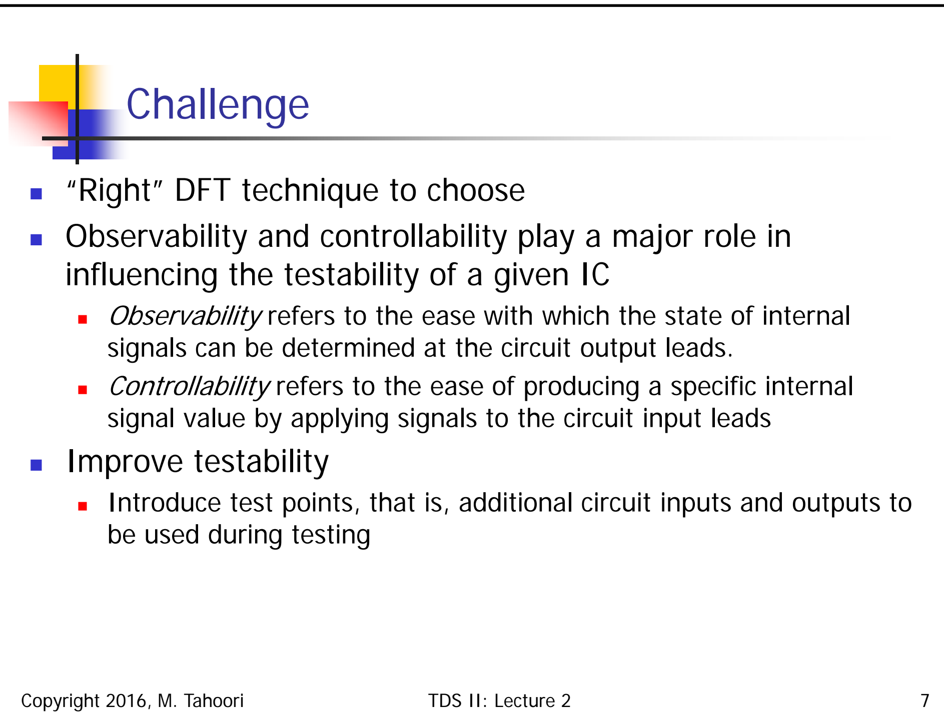
Challenge
"Right" DFT technique to choose
Observability and controllability play a major role in influencing the testability of a given IC
Observability refers to the ease with which the state of internal signals can be determined at the circuit output leads.
Controllability refers to the ease of producing a specific internal signal value by applying signals to the circuit input leads
Improve testability
Introduce test points, that is, additional circuit inputs and outputs to be used during testing
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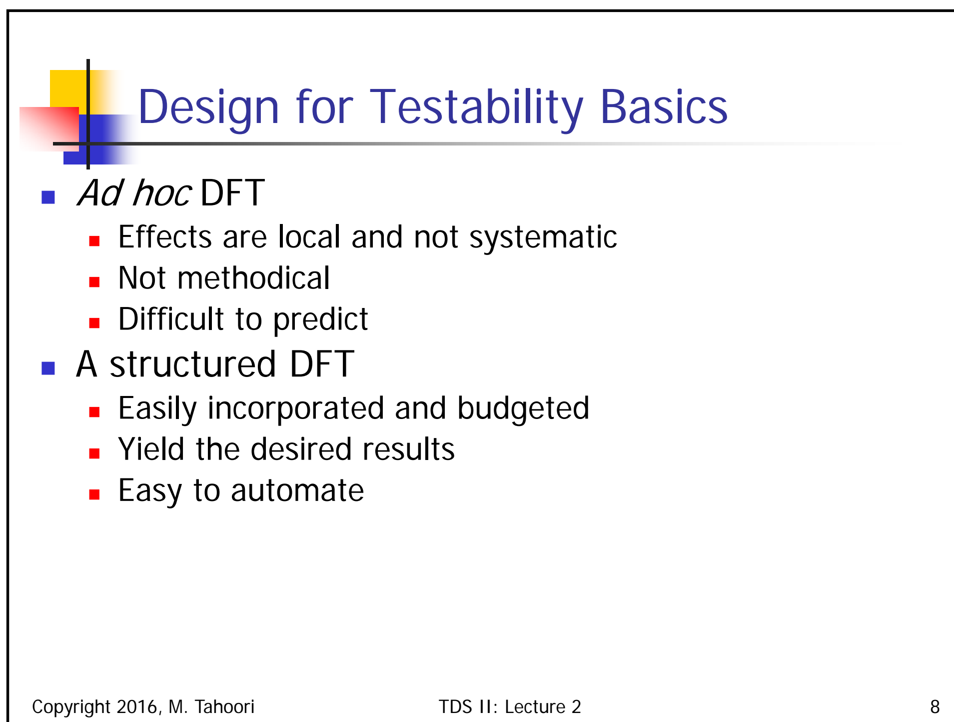
Design for Testability Basics
Ad hoc DFT
Effects are local and not systematic
Not methodical
Difficult to predict
A structured DFT
Easily incorporated and budgeted
Yield the desired results
Easy to automate
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Ad Hoc DFT Techniques
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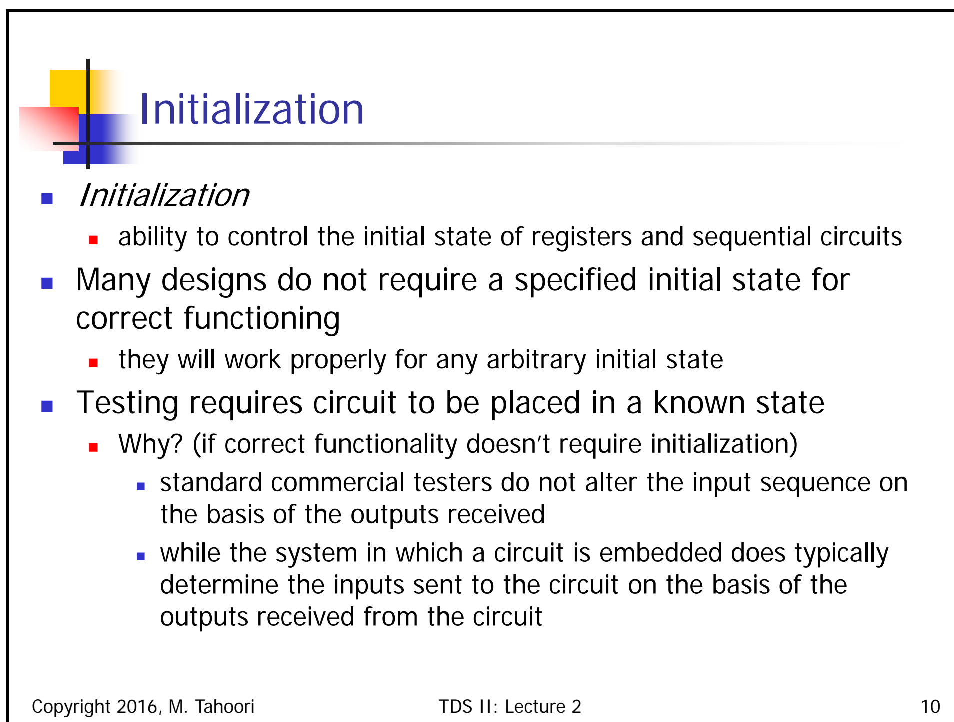
Initialization
Initialization
ability to control the initial state of registers and sequential circuits
Many designs do not require a specified initial state for correct functioning
they will work properly for any arbitrary initial state
Testing requires circuit to be placed in a known state
Why? (if correct functionality doesn't require initialization)
standard commercial testers do not alter the input sequence on the basis of the outputs received
while the system in which a circuit is embedded does typically determine the inputs sent to the circuit on the basis of the outputs received from the circuit
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Initialization

- Initialization Techniques
  - power-up reset (a)
  - tester reset (b)

Vdd R C CK 1D C1 Clear Q (a)

In CK 1D C1 Clear Q Tester input (b)

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Internal Resets

- Internal resets
  - Testability problem due to internal resets.
  - Possible solution

In CK 1D C1 Clear Q Logic CK 1D C1 Clear Q

In CK 1D C1 Clear Q Logic CK 1D C1 Clear Q + **Test Signal**

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Internal Clocks

- Designs contain flip-flops that are clocked by signals that are generated by some portions of the logic on the chip
- Solution
  - Substituting internal clocks by tester clock in test mode

Internal Clock
Tester Clock
0
1
MUX
Sel
Clock Signal
Test Mode

Gated Clocks

- Gated clocks to reduce power
  - Example of gated clock

In
1D
C1
Q
CK
&
Enable

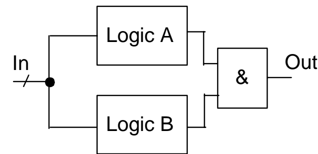
  - Possible solutions to the testability problem created by gated clocks

In
1D
C1
Q
CK
Enable
&
+
Test Enable

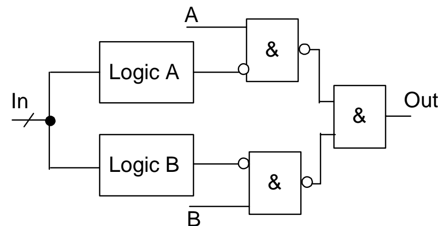
0
1
Mux
In
1D
C1
Q
CK

Logical Redundancy

- Test points to test redundant logic
  - Logical redundancy



  - Logic with test points A and B
    - A = B = 1
      - Normal operation
    - A = 1, B = 0
      - Test logic A



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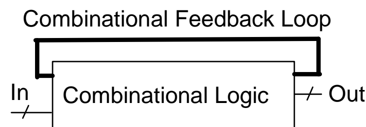
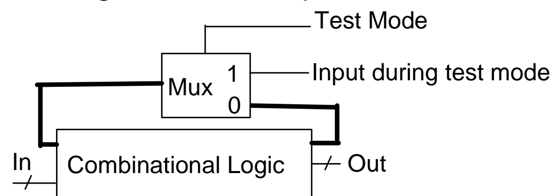
Combinational Feedback

- Circuits with combinational feedback loop.
  - Combinational feedback loop



  - Breaking feedback loop



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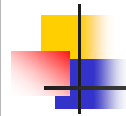

Summary: Ad-Hoc DFT Techniques

Feature	Ad hoc Technique
Unknown initial state	Initialization circuitry
Internal clock	Circuitry to disconnect internal clock and substitute tester clock
Logical redundancy	Avoid or add test points
Feedback loops	Circuitry to permit tester to break feedback loop
Internally generated signals for asynchronous set and Reset inputs of flip-flops	Circuitry to permit tester not to allow the tester not to allow these signals to set/reset flip-flops during test
Wired logic	Avoid
Bidirectional I/O pins	Circuitry to permit tester to configure them to operate in one direction
Tristate drivers and pass transistors	Circuitry to permit tester to configure them so that only 1 driver drives the bus

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