

## Master/Diploma Thesis

### “Memory Design for Energy Efficient Devices”

Energy efficient circuit design allows us to use integrated circuits for battery operated devices such as Internet of Things, implantable devices, and wearable devices. To achieve such energy efficiency, the supply voltage should be aggressively reduced which brings about different challenges to circuit design.

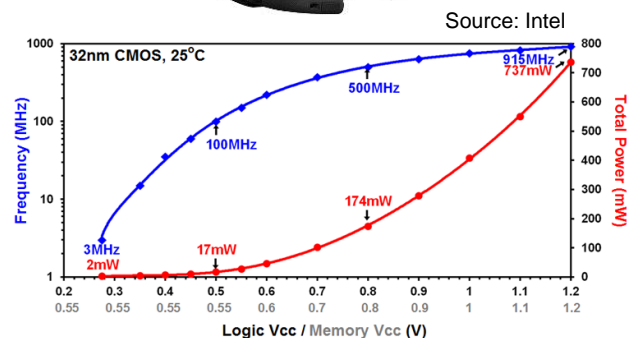
Nowadays, memories are dominating the overall chip components, therefore, energy efficient memory design is an important design step to enhance the overall energy efficiency. By reducing the supply voltage, memory arrays become less reliable and errors appear in different locations due to reduced noise margin. Therefore, it is imperative to study the behavior of memory arrays at low supply voltages.

#### Goals:

This thesis aims at developing a framework to estimate the characteristics of memory arrays at low supply voltage considering different variability sources. Our existing memory analysis framework is to be extended to account for energy efficiency. Afterwards, design space exploration will be performed using the same platform for the best possible memory design configuration.

#### Advantages for you:

- Learn about energy efficient techniques and memory architecture.
- Opportunity to work with industrial tools.



#### Required and helpful knowledge:

- C/C++ Programming, Digital Design, Basic knowledge of statistics

#### Supervisors:

Mohammad Saber Golanbari  
Rajendra Bishnoi  
Prof. Dr. Mehdi B. Tahoori

#### Contact person:

[golanbari@kit.edu](mailto:golanbari@kit.edu)

