


Testing Digital Systems I

Lecture 9: Boolean Testing Using Fault Models (D-Algorithm, PODEM)

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D Algorithm (More Examples)

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Example: A/0

- Step 1
 - D-Drive: Set A = 1

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Example: A/0

- Step 2
 - D-Drive : Set f = 0

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Example: A/0

- Step 3
 - D-Drive : Set $k = 1$

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Example: A/0

- Step 4
 - Consistency: Set $g = 1$

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Example: A/0

- Step 5
 - Consistency: $f = 0$
 - Already set

The diagram shows a logic circuit with inputs A, B, C, and D. Input A is marked with a red '1' and a cross, labeled 'sa0'. The circuit consists of several gates: an AND gate with inputs A and B (output e), an OR gate with inputs e and C (output f), an OR gate with inputs f and D (output h), an AND gate with inputs h and D (output k), and a NOT gate with input g (output 1). The final output L is the AND of k and the NOT of D. Red annotations show the current state: A=1, B=D, C=D, e=D, f=0, g=1, h=D, k=1, and L=D-bar.

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Example: A/0

- Step 6
 - Consistency: Set $c = 0$, Set $e = 0$

The diagram is identical to the one in Step 5, but with updated annotations for Step 6. Input C is now 0, and node e is now 0. All other nodes and the output L remain the same as in Step 5.

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Example: A/0

- Step 7
 - Consistency: Set $B = 0$
- Test found: $ABCD = 100X$

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Example s/1

- Primitive D-cube of Failure

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Example s/1

- Propagation D-cube for v

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Example s/1

- Forward & Backward Implications

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Example s/1

- Propagation D-cube for Z
- test found!

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Example: u/1

- Primitive D-cube of Failure

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Example: u/1

- Propagation D-cube for v

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Example: u/1

- Forward and backward implications

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Example: u/1

- Inconsistency
 - $d = 0$ and $m = 1$
 - cannot justify $r = 1$ (equivalence)
- Backtrack
 - Remove $B = 0$ assignment

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Example: u/1

- Backtrack
 - Need alternate propagation D-cube for v

The diagram shows a logic circuit with three inputs A, B, and C.

- Input A and B are connected to an AND gate (d, g) and an OR gate (k, m).
- Input C is connected to an AND gate (i, v) and an OR gate (l, u).
- Node m is connected to an AND gate (n, r) and an OR gate (p, q).
- Node r is connected to an AND gate (e, X) and an OR gate (f, s).
- Node s is connected to an AND gate (t, Y) and an OR gate (u, v).
- Node q is connected to an AND gate (p, q) and an OR gate (u, v).
- Node u is connected to an AND gate (l, u) and an OR gate (u, v).
- Node v is connected to an AND gate (i, v) and an OR gate (u, v).

 A red 'X' is placed over node u, and a red 'D' with a bar is placed next to node v. A red '1' is placed at node r and a red '0' is placed at node t.

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Example: u/1


- Propagation D-cube for v

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Example: u/1

- Propagation D-cube for Z

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Example: u/1

- Propagation D-cube for Z
- Implications
- Test Found!

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PODEM

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Motivation

- IBM introduced semiconductor DRAM memory into its mainframes – late 1970's
- Memory had error correction and translation circuits
 - To improved reliability
- D-ALG failed to generate test for these circuits
 - Search too undirected
 - Large XOR-gate trees
 - Must set all external inputs to define output
- Needed a better ATPG tool



PODEM -- Goel IBM (1981)


- Path Oriented DEcision Making
- New concepts introduced:
 - Expand binary decision tree only around primary inputs
 - This reduced size of tree from 2^n to $2^{\text{num_PI}}$
 - Use X-PATH-CHECK
 - To test whether D-frontier still there
 - D-Algorithm tends to continue intersecting D-Cubes
 - Even when D-Frontier disappeared
 - Objectives
 - bring ATPG closer to propagating D (\bar{D}) to PO
 - Backtracing
 - To obtain a PI assignment given an initial objective



Assigning Input Values (PODEM)

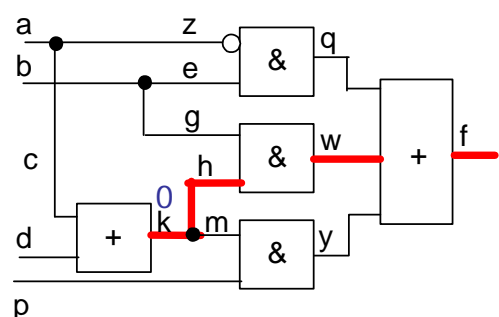
1. Assign value to an unassigned primary input
2. Determine all implications of assignment
3. If test is generated, exit; else
4. Is test is possible with additional input assignments ?
 - fault site doesn't have fault value assigned
 - Path of unassigned leads from D (\bar{D}) to an output
 - If yes, go to 1, if no
5. Change input assignments to untried combination, go to 2
 - If no untried combination exists — untestable fault

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Example: Test For k/1

- Put D' on k
 - D-Alg: assigned a D' to k and propagate it to output f
 - PODEM: try to justify 0 on k



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Example: Test For k/1

- Justify 0 on d
- Implication

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Example: Test For k/1

- K still hasn't D'
- Justify 0 on c
- Implication: $k=h=m=D'$

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Example: Test For k/1


- Propagate through w
- Set $g = 1$
- Implication

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Example: Test For k/1

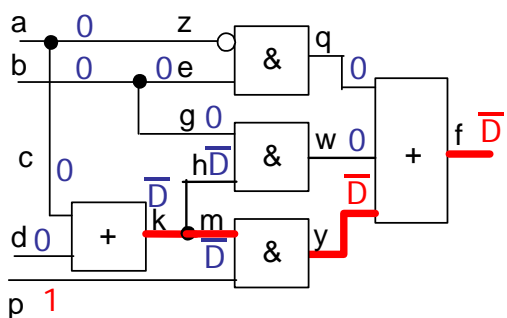
- Conflict
 - f is 1 so propagation is blocked
- Reverse the last assignment made to a PI
 - Set $b = 0$
- Implication

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Example: Test For k/1


- There is a propagation path from m to f
 - Set $p = 1$
- Implication
- Test found
 - $abcd = 0001$



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Another Example

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Example: S/1

- Select path s – Y for fault propagation

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Example: S/1

- Initial objective:
 - Set r to 1 to sensitize fault

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Example: S/1

- Backtrace from r

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Example: S/1

- Set A = 0 in implication stack

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Example: S/1

- Forward implications: $d = 0, X = 1$

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Example: S/1

- Initial objective: set r to 1

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Example: S/1

- Backtrace from r again

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Example: S/1

- Set B to 1.
 - Implications in stack: A = 0, B = 1

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Example: S/1

- Forward implications:
 - $k = 1, m = 0, r = 1, q = 1, Y = 1, s = \bar{D}, u = \bar{D}, v = \bar{D}, Z = 1$

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Example: S/1

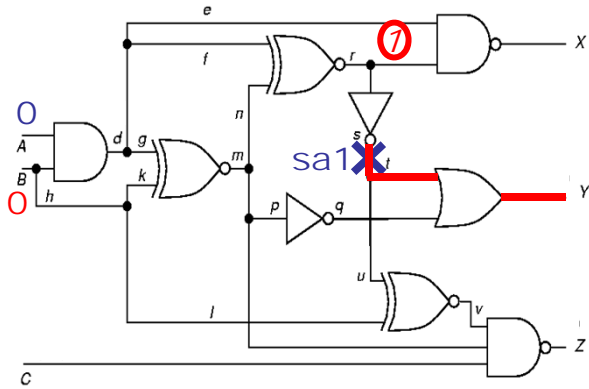
- X-PATH-CHECK
 - paths $s - Y$ and $s - u - v - Z$ blocked

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Example: S/1

- Set B = 0 (alternate assignment)



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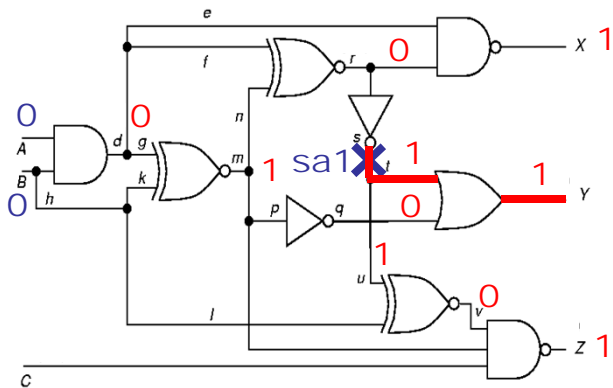
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43



Example: S/1

- Forward implications:
- d = 0, X=1, m = 1, r = 0, s = 1, q = 0, Y = 1, v = 0, Z = 1
- Fault not sensitized



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Example: S/1

- Set A = 1 (alternate assignment)

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Example: S/1

- Backtrace from r again

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Example: S/1

- Set $B = 0$.
- Implications in stack: $A = 1, B = 0$

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Example: S/1

- Forward implications:
 - $d = 0, X = 1, m = 1, r = 0$.
- Conflict: fault not sensitized. Backtrack

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Example: S/1


- Set B = 1 (alternative assignment)

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Example: S/1

- Forward implications:
 - $d = 1, m = 1, r = 1, q = 0, s = \bar{D}, v = \bar{D}, X = 0, Y = \bar{D}$
- Test found


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PODEM

- Major aspects
 - Which primary input should be assigned a logic value?
 - What value to assign to the selected primary input?
 - Determining inconsistencies in primary input assignments
 - Handling inconsistencies


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Which PI to Choose?

- Decision gate
 - Logic value at the output of a gate is such that only one input of the gate can control its output to the desired value
 - AND with output 0
- Imply gate
 - Logic value at the output of a gate is such that all inputs of the gate must be at a particular value in order to control its output to the desired value
 - AND with output 1
- To justify a logic value at the output of a decision gate, choose the "easiest" input.
 - The shortest logical path to primary inputs or has the best controllability
- To justify a logic value at the output of an imply gate, choose the "hardest" input
 - The longest logical path to primary inputs or has the worst controllability


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What Value to Assign?

- Path from the objective site to the selected primary input has an **even** number of inversions
 - Assign the same value to PI as the objective
- Path from the objective site to the selected primary input has an **odd** number of inversions
 - Assign the opposite value of the objective to PI

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Inconsistencies in PI Assignment

- After every primary input assignment, an implication step is performed.
- During implication, inconsistencies in primary input assignments are detected using the following rules:
 - If there are conflicting assignments at the same signal line of the network
 - If the logic value at the fault site doesn't activate the fault
 - If there is no path from the fault site to a primary output such that all side inputs of that path are either X or set at non-controlling values

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Handling Inconsistencies

- Backtracking
 - Flip the logic value at the primary input
 - Which was the last one to be assigned a value
 - Stack of primary inputs that have been assigned values
 - After flipping implication step is performed
 - No inconsistency detected
 - Continue
 - Otherwise
 - That primary input is removed from the stack and
 - X is assigned to that primary input
 - POP the next assigned PI from stack and repeat