Lecture 2: Types of Test

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Testing Principle

- Performed by
  - Automatic Test Equipment (ATE)
  - On-chip Built-In Self Test (BIST)
Tests for Manufacturing Defects

- **Chip**
  - Production Test
  - Wafer Sort or probe
    - Test Site
    - Die
  - Final Package
  - Burn In
  - Outgoing inspection
  - System Test
  - Incoming Inspection or Acceptance

- **Board**
  - In-Circuit or Bed-of Nails
  - Functional or Edge Connector

- **System**

Testing For Wearout Defects

- **On-Line Testing or Checking**
  - Concurrent checking techniques are designed to ensure that error is reported when the system produces incorrect outputs
  - Data Integrity
  - Techniques
    - Embedded Checkers - Error Detection
    - Periodic Diagnostic Programs
    - Watchdog Checks

- **Repair or Diagnostic Tests**
Testing For Transient Disturbances

- On-Line Testing or Checking
  - Embedded Checkers - Error Detection
  - Watchdog Checks

Important Observation

- Part can Operate Correctly with a Defective Component
  - Defect isn't Bad Enough to Prevent Correct Operation
    - CMOS gate-oxide short,
    - low $\beta$, ...
  
  **Can cause intermittent errors**

- Component is Redundant
Major Testing Categories

- Implicit
  - On-Line Test for Run-time Errors
    - Concurrent Checking, Monitoring, Built-in Test
- Explicit
  - Test for permanent defects
  - Referred to as “off-line testing” or simply “testing”

Implicit Testing

- Concurrent Checking, Monitoring, On-Line Test, Built-in Test
  - Test of operational system - Normal system inputs
  - Errors detected as they occur
  - Temporary as well as permanent faults
  - Identifies failed units for repair
- Circuit level techniques
  - Hardware faults detected
  - Prevents undetected data errors
- System level techniques
  - In Addition, Detect Control and Software Faults
    - Control flow checking
Implicit (Concurrent) Testing

- System level techniques
  - Memory Protection
  - Watchdog Timer
  - Watchdog Processor
    - Generalization of watchdog timer
    - Small processor operating in parallel with checked processor

- Circuit level techniques
  - Registers and Busses - parity code
  - RAM - Modified Hamming Code
  - Arithmetic Unit - Residue Code or Parity Prediction
  - Duplication
Temporary Failures

- Transient
  - Caused by environmental disturbances such as power-supply disturbances, electromagnetic interference, and radiation sources in space or terrestrial environments
  - Conductively Coupled - Supply voltage dip
  - Air coupled
    - Electromagnetic
    - Electrostatic

- Intermittent
  - Caused by flaws or latent manufacturing defects
  - Resulting in loss of noise margin, drive capability
    - Pattern sensitive faults

Explicit Testing

- Off-line test for permanent faults
  - Special test inputs used

- Output response analysis
  - Stored Response
  - Comparison (gold unit)
  - Compact Testing
    - Signature Analysis (LFSR)
Explicit Test Techniques

- **Parametric Test**
  - measures electrical properties of pin electronics
  - delay, voltages, currents, etc.
  - fast and cheap
  - Measure or "threshold" analog parameters
  - DC — Voltage levels, drive current, power,...
  - AC — Rise, fall, delay times

- **Boolean Test**
  - Digital test of logic operation
  - Also called functional test

- **Quasi-Boolean Test (AC test)**
  - Delay Fault Test

Explicit Tests According To Purpose

- **Characterization Test**
- **Production or Manufacturing Test**
- **Reliability (Accelerated Life) Test**
- **Stress Screen (Burn-In) Test**
- **Acceptance or Incoming Inspection**
- **Quality Test**
- **Repair, diagnosis, fault location**
Characterization Test

- Performed on new designs
- Measurement of Device Parameters and their Interactions
- performed on a sampled parts from different manufacturing lots
  - to account for process variation
- All Practical Combinations of
  - Supply Voltage
  - Temperature
  - Timing Conditions
  - Parametric Variations

- Shmoo Plot
- Used to
  - Set Final Specifications
  - Identify Areas to Improve Process to Increase Yield

Characterization Test (cont)

- Worst-case test
  - Choose test that passes/fails chips
  - Select statistically significant sample of chips
  - Repeat test for every combination of 2+ environmental variables
  - Plot results in Shmoo plot
  - Diagnose and correct design errors

- Less intensive characterization test performed during production life of chips to improve design and process to increase yield
Shmoo Plot

- Identify manufacturing defects.
- Identify areas where the manufacturing process steps (e.g., process optimization, wafer/batch monitoring parameters and procedures) and design characteristics (e.g., clock system design, timing critical paths) can be improved in order to increase yield.

Production Or Manufacturing Test

- Sort Out Defective Parts
- Bin Parts for Different Specifications
- Must cover high coverage of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Only checked whether the part will operate according to specification
- Both mechanical properties such as package seal, and the electrical properties must be tested
- Test at speed of application or speed guaranteed by supplier
Production Or Manufacturing Test

- **Chip**
  - Wafer Sort or Probe
    - done before wafer is scribed and cut into chips
    - Includes test site characterization
      - specific test devices are checked with specific patterns to measure:
        - Gate threshold
        - Polysilicon field threshold
        - Poly sheet resistance, etc.
  - Final Package test
  - IDDq
  - **Very-Low Voltage (VLV)** As a part of reliability test
  - Burn In
  - System test

Electrical Test During Wafer Sort

- **Gross Tests**
  - Test for gross defects, e.g., Iddq, pin leakage, opens, shorts, etc.
- **DC or Static Parametric Tests**
  - Measure voltage, current and power levels.
- **AC Parametric Tests**
  - Timing measurements of parameters such as propagation delay, setup and hold times.
- **Boolean Tests**
  - Ensure correct device logic behavior.
- **Semi-Boolean (Delay) Tests**
  - Ensure path delays are within specifications.
**Production Or Manufacturing Test**

- Board
  - Bare Board
  - In-Circuit or Bed-of Nails
  - Functional or Edge Connector

**Reliability (Accelerated Life) Test**

- Test to Estimate Time to Failure in Normal Operation
  - Part is tested after high temperature and high voltage stress
  - Attention is paid so that the lifetime of defect-free parts is not significantly degraded due to stresses
Stress Screen (Burn-in) Test

- Some chips that pass production test will fail very quickly thereafter
- Process:
  - Subject chips to high temperature & over-voltage supply, while running production tests
    - 40% above normal supply voltage, temperature above 100 C, time of 30 hours
    - forcing failure in these "weak" chips
- Catches:
  - Infant mortality cases (short burn-in time required)
    - these are damaged chips that will fail in the first 2 days of operation - causes bad devices to actually fail before chips are shipped to customers
  - Freak failures (long burn-in time required)
    - devices having same failure mechanisms as reliable devices

Acceptance Or Incoming Inspection

- Test to Determine Degree of Compliance with Purchaser's Requirements
- Can be:
  - Similar to production testing
  - More comprehensive than production testing
  - Tuned to specific systems application
- Often done for a random sample of devices
  - Sample size depends on device quality and system reliability requirements
  - Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost
Quality Test

- Sample of Each Lot Tested
- Used by Quality Assurance Department
- Estimates Quality Level of Manufactured Parts

Repair, Diagnosis, Fault Location

- Test to Locate Failure Site on Failed Part
  - Board or boards in system
  - Chip or chips on board
  - Net on chip

- Purpose
  - Return system or board to correct operation
  - Improve chip yield, reliability, quality
Repair, Diagnosis, Fault Location

Software Diagnosis Techniques

- Fault simulation => probable fault location
- Pre-calculated fault dictionaries
- Post-test fault simulation

Hardware Diagnosis Techniques

- Direct observation
  - place chip in failed state
  - observe image
    - light emission
    - thermal effects
    - focused electron beam interaction
- Measure chip response to outside physical stimulus
  - scan chip with laser, electron beam, ion beam
  - monitor chip I/O, power supply

Limitations

- Defect dependent
- Some defects don't emit light or cause heating
- Needs access to chip transistors and internal wiring
Repair, Diagnosis, Fault Location

- Deprocessing
  - Remove chip layers until defect is isolated
    - ultra-fine probes
    - microscopes
      - optical, scanning-electron, scanning-probe

Testing Taxonomy

- Testing
  - Design Verification
  - Explicit Testing
  - Implicit Testing
    - Or
    - On-line Testing
  - Characterization
  - Production Test
  - Reliability Test
  - Qualification
  - Diagnosis

- Wafer Sort
  - Package Test
  - IDDQ
  - VLV
  - Burn-in
  - Min Vdd
  - SHOVE
  - System Test

- Gross Test
  - DC parametric Test
  - AC parametric Test
  - Boolean Test
  - Quasi-Boolean (Delay) Test
### Types of Test

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<tr>
<th>Type of Test</th>
<th>Description</th>
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<tbody>
<tr>
<td><strong>Production Test</strong></td>
<td>Tests to sort out defective manufactured parts</td>
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<tr>
<td><strong>Wafer Sort or Probe</strong></td>
<td>Test of each die while still on the wafer</td>
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<tr>
<td><strong>Final or Package Test</strong></td>
<td>Test of packaged chips and separation into classes or bins (military,</td>
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<td>commercial, industrial)</td>
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<td><strong>Acceptance Test</strong></td>
<td>A test to demonstrate the degree of compliance of a device with</td>
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<td></td>
<td>purchaser’s requirements</td>
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<tr>
<td><strong>Sample Test</strong></td>
<td>Test of some but not all parts</td>
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<tr>
<td><strong>Go / No Go Test</strong></td>
<td>Test to determine whether device meets specification</td>
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<tr>
<td><strong>Characterization</strong></td>
<td>Test to determine actual values of device AC and DC parameters and</td>
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<td>the interaction of parameters. Used to set final specifications and to</td>
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<td>identify areas to improve process to increase yield.</td>
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<tr>
<td><strong>Stress Screening</strong></td>
<td>Test with stress (high temperature, temperature cycling, voltage, vibration,</td>
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<td>etc.) applied to eliminate short life parts</td>
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<tr>
<td><strong>Reliability Test (Accelerated Life Test)</strong></td>
<td>Test after subjecting the part to extended high temperature or voltage to estimate time to failure in normal operation</td>
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<tr>
<td><strong>Diagnostic Test</strong></td>
<td>Test to locate failure site on failed part</td>
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<tr>
<td><strong>Quality Test</strong></td>
<td>Test by quality assurance department of a sample of each lot of manufactured parts. More stringent than final test.</td>
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<tr>
<td><strong>On-line Test</strong></td>
<td>On-line testing to detect errors that occur during normal system operation.</td>
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<tr>
<td><strong>System Test</strong></td>
<td>Test by plugging a device into an actual system and running the system.</td>
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<tr>
<td><strong>Design Verification</strong></td>
<td>Verifying the correctness of a design</td>
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### Test Flow

1. **Die**
   - DC Parameters
   - Functional
   - I/O
   - Logic
   - Delay

2. **Wafer Sort**
   - GO/No-GO
   - In-line Wafer Tests

3. **Manufacturing**
   - Masks

4. **Packaged Device**
   - Burn-In
   - Package Test
   - Test escapes
   - Customer
   - System Integration
   - System Test

5. **Test Flow**
   - Customer
   - Test escapes
   - Incoming inspection
   - Fallout

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