Testing Digital Systems I

Lecture 1: Introduction

Instructor: M. Tahoori

Today’s Lecture

- Logistics
- Course Outline
- Introduction
Logistics

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- Lecture:
  - When: Thursdays 15:45-17:15
  - Where: Multimedia HS -101, Building 50.34

Logistics (cont)

- Requirements
  - Logic Design
  - Computer Architecture
  - Background on
    - Algorithms and Programming
    - Hardware description languages (VHDL or Verilog)
Reference Books

- **Textbook**

- **Recommended**

Course Outline

- **Basics**
- Test generation methods
- Design for Testability (DFT)

- I try to be flexible. The order and contents may be changed as we proceed.
Outline: Basics

- Introduction
- Failures and errors
- Fault models
- Functional vs Structural testing

Outline: Test Generation

- Test generation techniques and algorithms for combinational logic
- Essentials of test generation methods for sequential circuits
- Logic and fault simulation
Outline: Design For Testability (DFT)

- Ad hoc DFT techniques
- Internal scan design
- Boundary scan

Introduction
Definitions

- Design synthesis:
  - Given an Input-Output function, develop a procedure to manufacture a device using known materials and processes

- Verification:
  - Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given Input-Output function
Design Steps

- Specifications
- High-level Description
- Functional Description
  - Behavioral VHDL, C
  - Structural VHDL

Design Steps (cont)

- Specifications
- High-level Description
- Functional Description
- Placed & Routed Design
- Gate-level Design
- Logic Description
  - X = (A(B+C)) + (A+D) + (A(B+C))
  - Y = (A(B+C)+A+C+D+A(BC+D))
Testing

- The process of determining whether a piece of device
  - Is functioning correctly, or
  - Is defective (broken or faulty)
- Equipment can be defective because it doesn't function
  - as designed, or
  - as specified

Testing (cont)

- The need for test depends on
  - Process yield, Y,
    - the proportion of finished units that are not defective
    - Depends on maturity of the manufacturing process, size of the integrated circuit chips and the characteristics of the implemented design, etc.
  - Acceptable quality level (AQL)
    - the planned minimum fraction of defective shipped units
    - Defective Parts per Million (DPM)
    - Depends on the volume of the product, criticality of the applications and the cost of the parts
Yield and Quality Level

- Y and AQL are rarely exactly known
  - Statistically estimated
  - Not feasible to thoroughly test all parts
- Process yield is typically less than AQL
  - Defective units must be identified and removed so as to increase the percentage of good units shipped to the customer.

Testing Process

Testing as Filter Process

Good chips
\[ \text{Prob(good)} = y \]

Fabricated chips

Defective chips
\[ \text{Prob(bad)} = 1 - y \]

Prob(pass test) = high

Mostly good chips

Overkill Escapes

Test (yield loss)

Mostly bad chips

A Part Fails to Operate

- Design Does Not Correspond to Specification
  - Logic Design Incorrect
  - Physical Design Incorrect

- Physical Part Does Not Correspond to Design
  - Manufacturing Defect Present
  - Wear Out Defect Present

- External or Environmental Disturbance
  - Transient Disturbance
  - Power or Temperature Specification Violated
Logic Design Verification

- Specification
  - Behavioral or Register Transfer
  - Table of Combinations – Boolean Function
  - Sequential Circuit or State Machine Flow Table
  - Simulation Vectors and Responses
  - Informal Word Description of Functionality

- Verification Technique
  - Synthesis
  - Matching of Two Design Paths
  - Simulation — Emulation
  - Formal Verification

Verification vs. Test

- Verifies correctness of design.
  - Performed by simulation, hardware emulation, or formal methods.
  - Performed once prior to manufacturing.
  - Responsible for quality of design.

- Verifies correctness of manufactured hardware.
  - Two-part process:
    - 1. Test generation: software process executed once during design
    - 2. Test application: electrical tests applied to hardware
  - Test application performed on every manufactured device.
  - Responsible for quality of devices.
Problems of Ideal Tests

Definition
- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.

Problems
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects.
- Unacceptable test costs
  - Test generation effort, test application time

Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected
  - The fraction (or percentage) of such chips is called the yield loss.
- Some bad chips pass tests
  - The fraction (or percentage) of bad chips among all passing chips is called the defect level.
VLSI Technology and Trends

- These trends impact cost and difficulty of testing

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Costs of Testing

- **Design for testability (DFT)**
  - Chip area overhead
  - Yield reduction
  - Performance overhead

- **Software processes of test**
  - Test generation
  - Fault simulation
  - Test programming and debugging

- **Manufacturing test**
  - *Automatic test equipment (ATE)* capital cost
  - Test center operational cost
Example: Cost of Testing

- 0.5-1.0GHz, analog instruments, 1,024 digital pins:
  - ATE purchase price
    - \(= \$1.2M + 1,024 \times \$3,000 = \$4.272M\)
  - Running cost (five-year linear depreciation)
    - \(= \text{Depreciation} + \text{Maintenance} + \text{Operation}\)
    - \(= \$0.854M + \$0.085M + \$0.5M\)
    - \(= \$1.439M/\text{year}\)
  - Test cost (24 hour ATE operation)
    - \(= \$1.439M/(365 \times 24 \times 3,600)\)
    - \(= 4.5 \text{ cents/second}\)
  - Digital ASIC test time: 6 seconds or 27 cents

Cost of Manufacturing Test

Source: International Technology Roadmap for Semiconductor Industry (ITRS)
Roles of Testing

- **Detection:**
  - Determination whether or not the *device under test* (DUT) has some fault.
- **Diagnosis:**
  - Identification of a specific fault that is present on DUT.
- **Device characterization:**
  - Determination and correction of errors in design and/or test procedure.
- **Failure mode analysis (FMA):**
  - Determination of manufacturing process errors that may have caused defects on the DUT.

Who Needs to Take This Class?

- **Testing (Test & DFT Engineer):**
  - Needs to focus on all topics,
  - More emphasize on test flow and tools
- **Design automation (CAD Engineer):**
  - Focus on test generation and DFT algorithms
    - Test automation
- **Circuit design and computer architecture (Designer):**
  - Focus on DFT techniques
    - Testable designs
  - Interaction of test flow and design flow
    - How DFT affect the original design